EK-HSC50-SV-002

HSC50

SERVICE MANUAL

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EK-HSC50-SV-002

HSC50
Service Manual

Prepared by Educational Services

of

Digital Equipment Corporation

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PREFACE

This manual describes the HSC50 subsystem for use by field service representatives. It includes such topics as HSC50 controls and indicators, field replaceable units, problem analysis, and diagnostic procedures.

All information in this manual is informational/instructional and is designed to assist field service personnel with HSC50 maintenance. Operational theory is included wherever such background can be helpful to field service. A glossary of HSC50-related terminology is located at the back of this document.

Detailed descriptions of HSC50 utilities and diagnostics are not included in this document. Installation procedures are also described in another manual. For source material on these and other subjects not within the scope of this manual, refer to the list of related documentation at the end of Chapter 1.

NOTE

This document supersedes the *HSC50 Service Manual* (EK-HSC50SG-001) and replaces the *HSC50 Maintenance Guide* (AA-P672A-TK).

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This chapter includes general information about the HSC50 Mass Storage Server including:

- Subsystem block diagrams
- Packaging and logic module descriptions
- Maintenance features
- Physical specifications
- Related documentation

1.2 GENERAL INFORMATION

Defined as a disk and/or tape subsystem, the HSC50 can interface to multiple hosts using the Computer Interconnect (CI) bus. In case of bus failure, two CI buses are included with the subsystem. Refer to Figure 1-1 for a sample 5-node cluster configuration utilizing two HSC50s and three host computers. All three hosts access both HSC50s over the CI bus and, through dual-porting, both HSC50s can access the tape formatter and the disks.

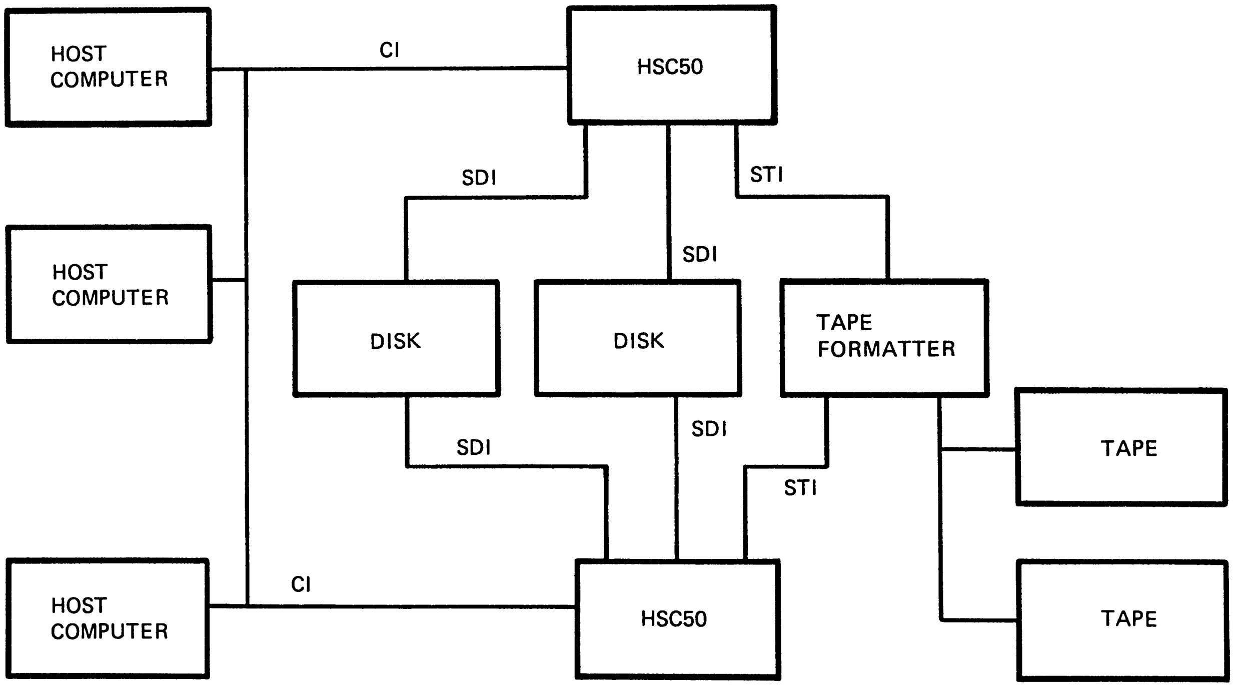


Figure 1-1 Redundant HSC50 System

The HSC50 supports a combination of six disk and tape data channels. Each disk data channel supports four drives over the Standard Disk Interface (SDI). Each tape data channel supports four tape formatters over the Standard Tape Interface (STI). Each formatter supports four tape transports.

Consult the HSC50 software release notes for the maximum number of tape formatters conforming to the STI bus. These software release notes are shipped with each HSC50 and with updates of the software.

1.2.1 Packaging, Cooling, and Power

HSC50 logic and power systems are housed in a modified H9642 cross-products cabinet with both front and rear access (Figure 1-2).

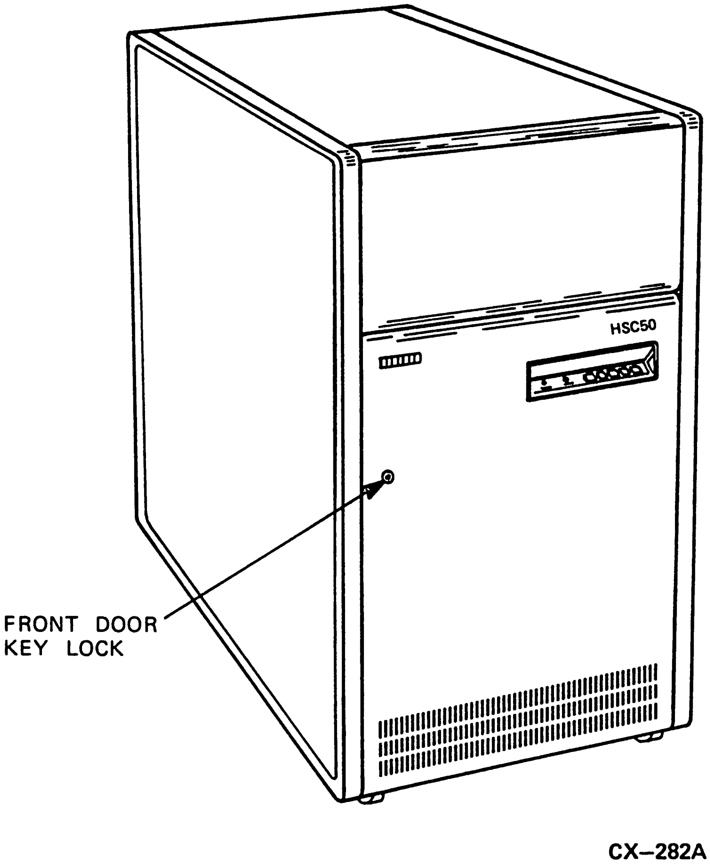


Figure 1-2 HSC50 Cabinet – Front

On the front of the cabinet are the operator control panel switches and indicators. Switch operation and indicator functions are described in Chapter 2.

To access the cabinet interior, open the front door with a key (cabinet lock assembly part number 12-14664). Located on the back of the front door are two TU58 drives, the TU58 run indicators, and slots for tape storage (Figure 1-3).

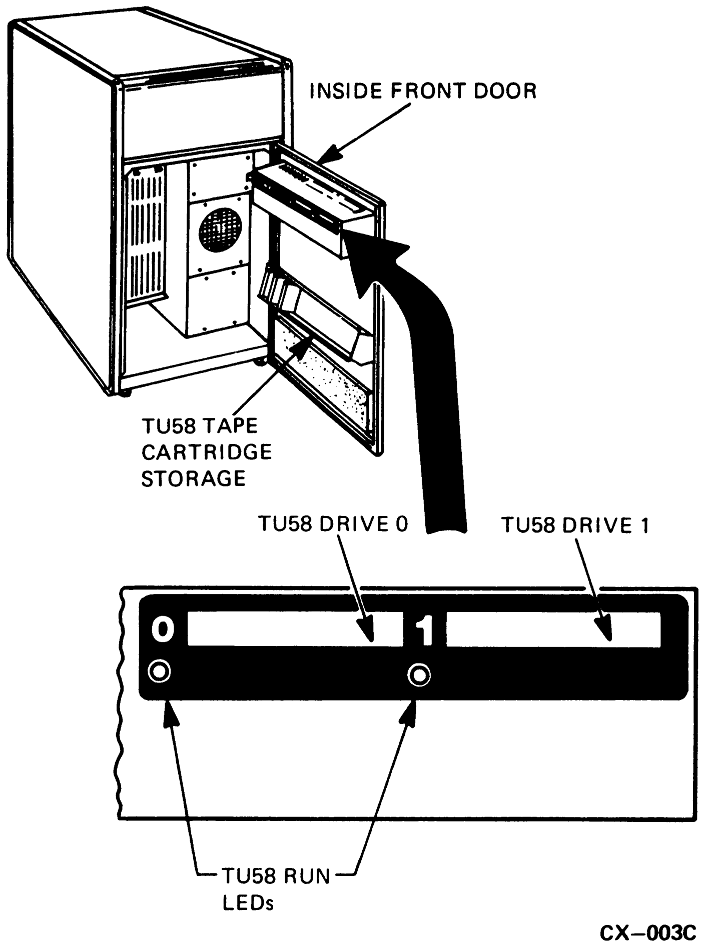


Figure 1-3 HSC50 – Inside Front View

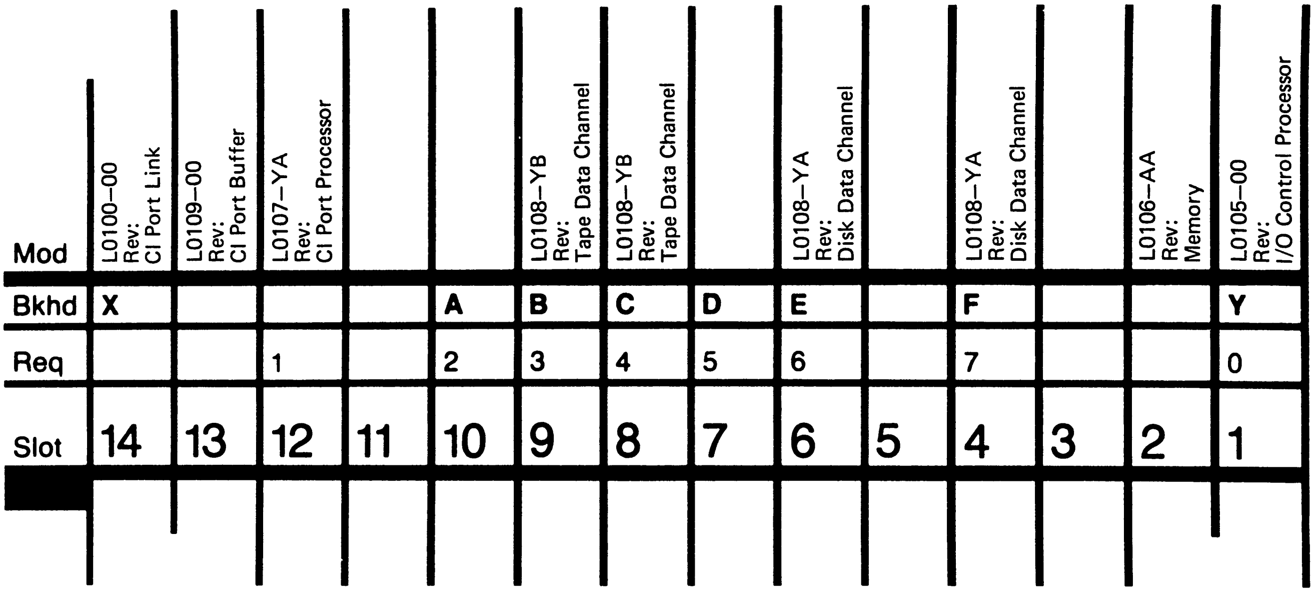
A 14-slot card cage with a corresponding backplane provides housing for the HSC50 logic modules (L-series extended hex). When viewed from the front, the card cage and backplane occupy the lower left of the cabinet. Above the card cage is a module utilization label indicating the slot location of each module (Figure 1-4). All unassigned slots contain baffles.

NOTE

All requestor slots A through F, illustrated in Figure 1-4, are optional tape or disk data channels.

The upper right-hand portion of the cabinet houses the maintenance access panel. A dc power on/off switch and connectors for the TU58, the operator control panel, and the maintenance terminal port are located on this panel.

Power supply units are housed underneath the maintenance panel. A basic HSC50-AA/AB contains one power supply capable of providing power for three data channels. A fourth data channel requires the addition of an auxiliary power supply. Each power supply has a fan drawing air from the front of the cabinet across the power unit and exhausting it through a rear duct.



Mod	L0100–00 Rev: CI Port Link	L0109–00 Rev: CI Port Buffer	L0107–YA Rev: CI Port Processor			L0108–YB Rev: Tape Data Channel	L0108–YB Rev: Tape Data Channel		L0108–YA Rev: Disk Data Channel		L0108–YA Rev: Disk Data Channel		L0106–AA Rev: Memory	L0105–00 Rev: I/O Control Processor
Bkhd	X				A	B	C	D	E		F			Y
Req			1		2	3	4	5	6		7			0
Slot	14	13	12	11	10	9	8	7	6	5	4	3	2	1

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Figure 1-4 HSC50 Module Utilization Label Example

Figure 1-5 shows the back of the HSC50 cabinet. The rear door is opened with a 5/32-inch hex wrench.

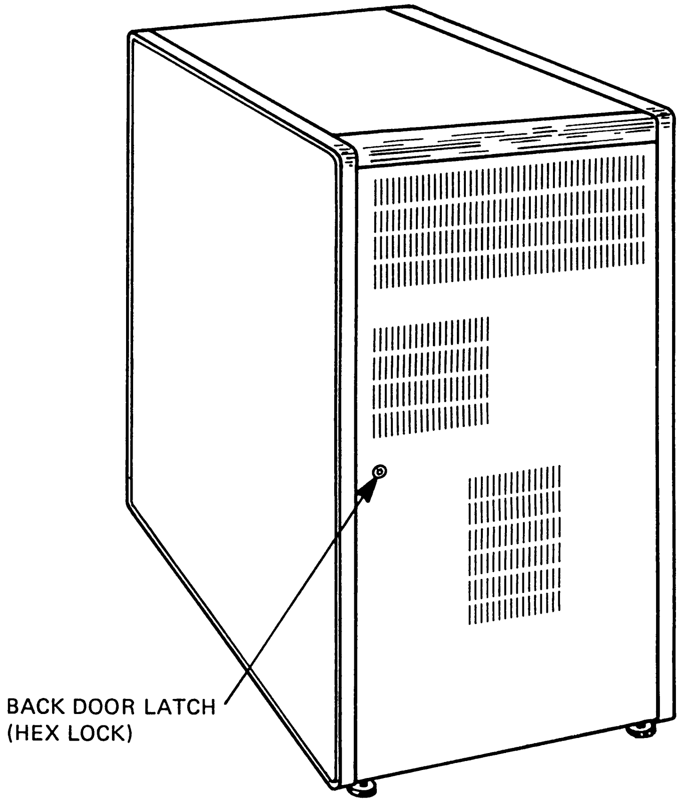

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Figure 1-5 HSC50 Cabinet – Rear

Logic modules are cooled by a blower mounted behind the card cage (Figure 1-6). Air is drawn in through the front door louver, up through the modules, and exhausted through the middle duct at the back.

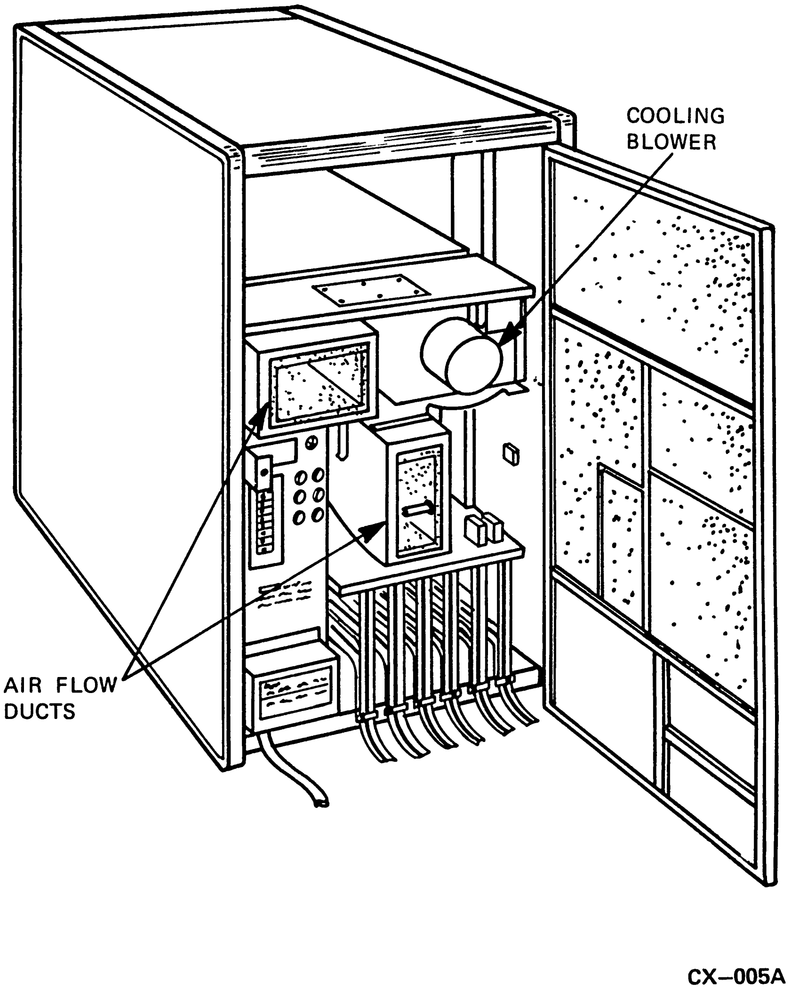


Figure 1-6 HSC50 – Inside Rear View

Two levels of cable connections are found in the HSC50: backplane to bulkhead and bulkhead to outside the cabinet. All connections to the logic modules are made via the backplane. All cables attach with press-on connectors to the backplane.

The power controller is in the lower left-hand rear corner of the HSC50. Also at the rear of the HSC50, the power control bus and delayed output line are connected to noise isolation filters.

Exterior CI, SDI, and STI buses are shielded up to the HSC50 cabling bulkhead. These cables are attached to bulkhead connectors located at the bottom rear of the cabinet.

From the interior of the I/O bulkhead connectors, unshielded cables are routed to the backplane and are attached with press-on connectors.

1.2.2 External Interfaces

Figure 1-7 shows the external hardware interfaces used by the HSC50.

External interface lines include:

- **CI Bus** – Four coaxial cables: two-path serial bus with a transmit and receive cable in each path; the bus for communication between system host(s) and the HSC50.
- **SDI Bus** – Four shielded wires for serial communication between the HSC50 and disk drives (one SDI cable per drive per controller).
- **STI Bus** – Four shielded wires for serial communication between the HSC50 and tape formatters (one STI cable per formatter).
- **Serial Line Interface** – RS-232-C cable for auxiliary terminal communication with the I/O control processor module.
- **Serial Line Interface** – RS-232-C cable linking the TU58 controller to the HSC50.

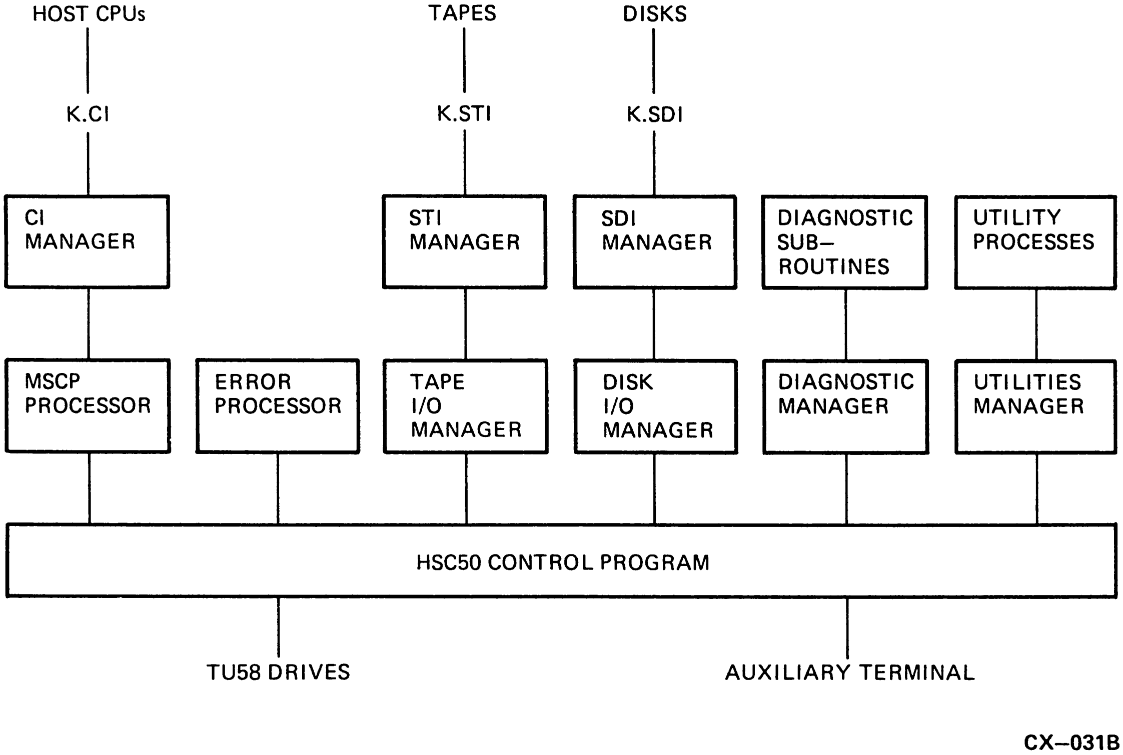


Figure 1-7 HSC50 External Interfaces

1.2.3 Internal Software

Major HSC50 software modules operating internally are shown at a block level in Figure 1-8. Each software module is described in the subsequent paragraphs.

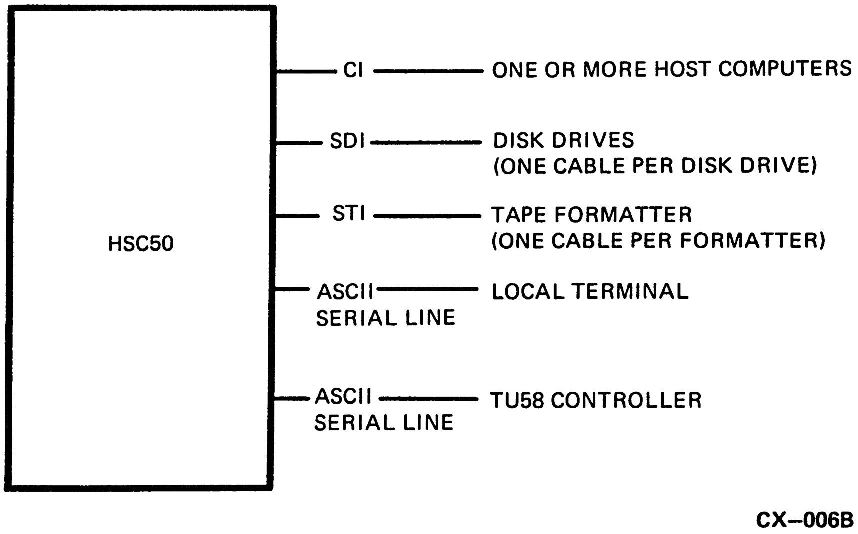


Figure 1-8 HSC50 Internal Software

1.2.3.1 HSC50 Control Program – The HSC50 control program (found on the System tape) is the lowest level manager of the subsystem. It provides a set of subroutines and services shared by all HSC50 processes. This program performs the following functions:

- Initializing and reinitializing subsystem functions
- Managing the TU58 local storage media
- Executing all auxiliary terminal I/O
- Scheduling processes (both functional and diagnostic) for execution by the P.ioc

Functional processes within the HSC50 communicate with the HSC50 control program. They communicate through shared data structures and send/receive messages.

1.2.3.2 CI Manager – The CI manager is responsible for handling low-level CI packet exchanges.

1.2.3.3 MSCP Processor – The MSCP processor is responsible for validating, interpreting, and routing incoming MSCP commands and dispatching MSCP completion acknowledgments.

1.2.3.4 Tape I/O Manager – The tape I/O manager sets up the data transfer structures for tape operations and manages the physical positioning of the tape.

1.2.3.5 STI Manager – The STI manager handles the STI protocol, responds to attention conditions, and manages the online/offline status of the tape drives.

1.2.3.6 Disk I/O Manager – The disk I/O manager performs the following:

- Translates logical disk addresses into drive-specific physical addresses
- Organizes the data-transfer structures for disk operations
- Manages the physical positioning of the disk heads

1.2.3.7 SDI Manager – The SDI manager performs the following:

- Handles the SDI protocol
- Responds to attention conditions
- Manages the online/offline status of the disk drives

1.2.3.8 Error Processor – The error processor responds to all detected error conditions. It reports errors to the diagnostic manager and attempts to recover from errors (ECC, bad-block revectoring, retries, etc.). When recovery is not possible, a diagnostic is run to determine if the subsystem can continue to function without the failing resource. Then appropriate action is taken to remove the failing resource or to terminate subsystem operation.

1.2.3.9 Diagnostic Manager – The diagnostic manager is responsible for automatic diagnosis, for error reporting, and for error logging. It also provides decision making and diagnostic sequencing functions and can access a large set of resource-specific diagnostic subroutines.

1.2.3.10 Utilities Manager – The utilities manager performs the following functions:

- Interpreting incoming utility requests
- Setting up the appropriate subsystem environment for operation of the requested utility
- Invoking the utility process
- Returning the subsystem to its normal environment upon completion of the utility execution

1.2.3.11 Utility Processes – The set of utility processes perform volume-management functions (such as formatting, disk-to-disk copy, disk-to-tape copy, tape-to-disk restore). It also handles miscellaneous operations required for modifying subsystem parameters or for analyzing subsystem problems (such as TU58 copy, TU58 patch, and error dump).

1.2.4 Subsystem Block Diagram

The HSC50 is a multimicroprocessor subsystem with two shared memory structures, one for control and one for data. In addition, the HSC50 I/O control processor fetches its own instructions from a private (program) memory. Figure 1-9 shows an HSC50 block diagram and its position in the subsystem. Each major block is a module, unless otherwise specified.

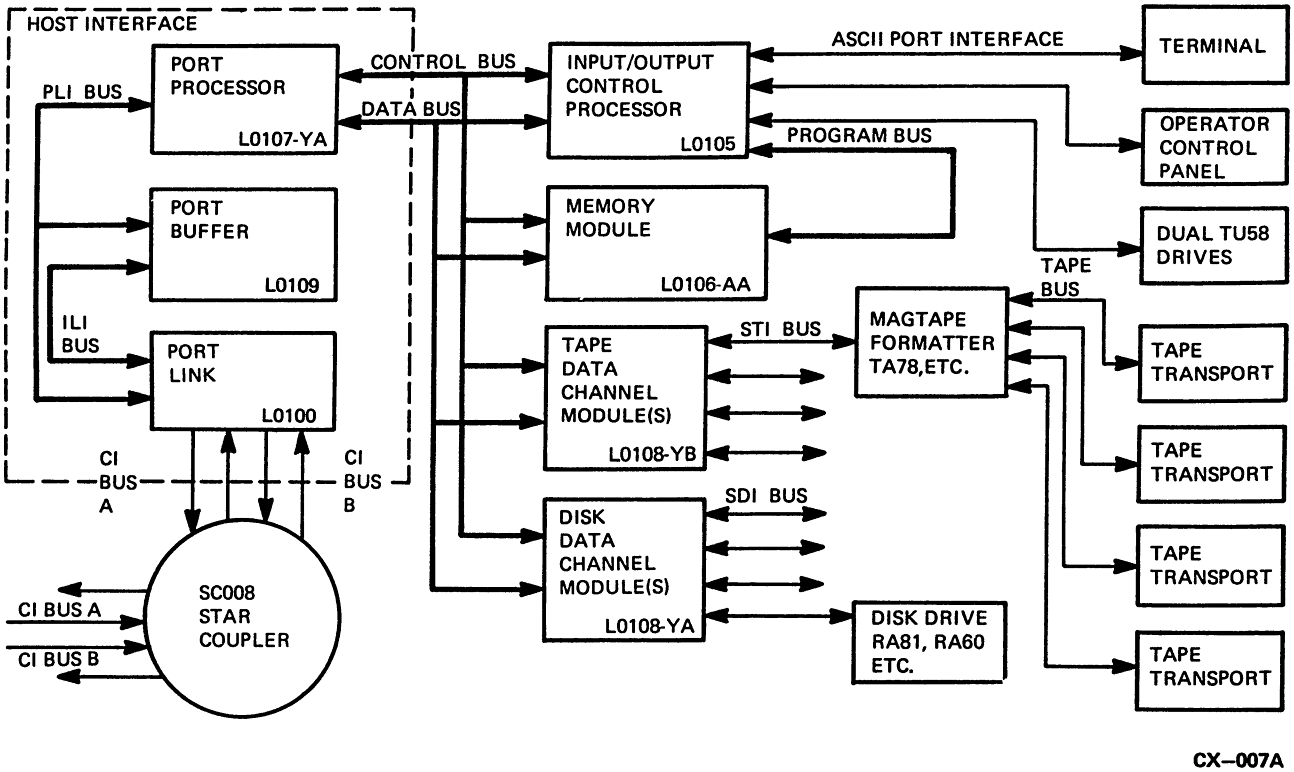


Figure 1-9 Subsystem Block Diagram

1.3 MODULE DESCRIPTIONS

This section describes each of the HSC50 logic modules.

References to modules by their engineering terms appear throughout HSC50 documentation, as well as on diagnostic printouts. For this reason, the the engineering term is shown in parentheses after the formal name for each module. These relationships are also indicated in Figure 1-9.

1.3.1 Port Link Module (LINK) Functions

The port link module (L0100), a part of the Host Interface Module Set (K.ci). performs the following functions:

- Serialization/deserialization, encoding/decoding, dc isolation

  Information transmitted over the CI bus is serialized and Manchester encoded. This encoding scheme permits transmission of a self-clocking data stream over the CI. The driver circuit includes a transformer for ac coupling the encoded signal to the coaxial cable. Information received from a CI transmission is decoded and converted to bit-parallel form. The circuitry also provides carrier-detection for determining when the CI is in use by another node.

- Cyclic redundancy check (CRC) generation/checking

  A 32-bit CRC character is generated and appended to a message packet. When a packet transmission is received, the CRC is checked. An incorrect CRC means either errors were induced by noise or a packet collision occurred.

- ACK/NAK generation

  Upon receipt of a packet addressed to the LINK, an ACK is generated if the following conditions exist:

  - Error-free CRC
  - Buffer space available for the message

  Upon receipt of a packet addressed to this node, a NAK is generated if the following conditions exist:

  - Error-free CRC
  - No buffer space available for the message

  No response is made if a packet addressed to this node is received with CRC error.

- Packet transmission

  Transmitter logic performs the following functions:

  - Executes the CI arbitration algorithm
  - Transmits the packet header
  - Moves the stored information from the transmit packet buffer to the Manchester encoder
  - Calculates the CRC and appends it to the end of the packet
  - Receives the expected ACK packet

- Packet reception

  Receiver logic performs the following functions:

  - Detects the start of the CI transmission
  - Detects the sync characters
  - Decodes the packet header information
  - Checks the CRC
  - Moves the data from the Manchester decoder
  - Returns the appropriate ACK packet

The port link module interfaces via line drivers/receivers directly to the CI coaxial cables. On the HSC50 interior side, the port link module interfaces to the port buffer module through a set of Interconnect Link (ILI) interface signals.

1.3.2 Port Buffer Module (PILA) Functions

The port buffer module (L0109) provides a limited number of high-speed memory buffers to accommodate the difference between the burst data rate of the CI bus and HSC50 internal memory buses. It also interfaces to the port link (CI link) module via the ILI signals and the port processor module via port/link interface (PLI) signals.

1.3.3 Port Processor Module (K.pli) Functions and Interfaces

The port processor module (L0107-YA) functions are:

- Executing and validating low-level CI protocol
- Moving command/message packets to/from HSC50 control memory
- Moving data packets to/from HSC50 data memory

The port processor module interfaces to three buses:

- The PLI bus interfaces the port buffer and port link modules
- The control memory bus interfaces HSC50 control memory
- The data memory bus interfaces HSC50 data memory

1.3.4 Disk Data Channel Module (K.sdi) Functions

Disk data channel module (L0108-YA) operation is controlled by an onboard microprocessor with a local programmed read-only memory (PROM). Functions of this module are:

- Transmits control and status information to the disk drives
- Monitors real-time status information from the disk drives
- Monitors in real time the rotational position of all the disk drives attached to it
- Transmits data between HSC50 data memory and the disk drives
- Generates and compares error correction code (ECC) and error detection code (EDC) during data transfers

Commands and responses pass between the disk data channel microprocessor and other internal HSC50 processes through control memory. The disk data channel module interfaces to the control memory bus and to the data memory bus. It can also interface to four disk drives with four individual SDI buses. Currently, combinations of up to six tape data channel or disk data channel modules are possible in the HSC50. Configuration guidelines are found in the *HSC50 Installation Manual*.

1.3.5 Tape Data Channel Module (K.sti) Functions

Tape data channel module (L0108-YB) operation is controlled by an onboard microprocessor with a local programmed read-only memory (PROM). It performs the following functions:

- Transmits control and status information to the tape formatters
- Monitors real-time status information from the tape formatters
- Transmits data between the data memory and the tape formatters
- Generates and compares the EDC during data transfers

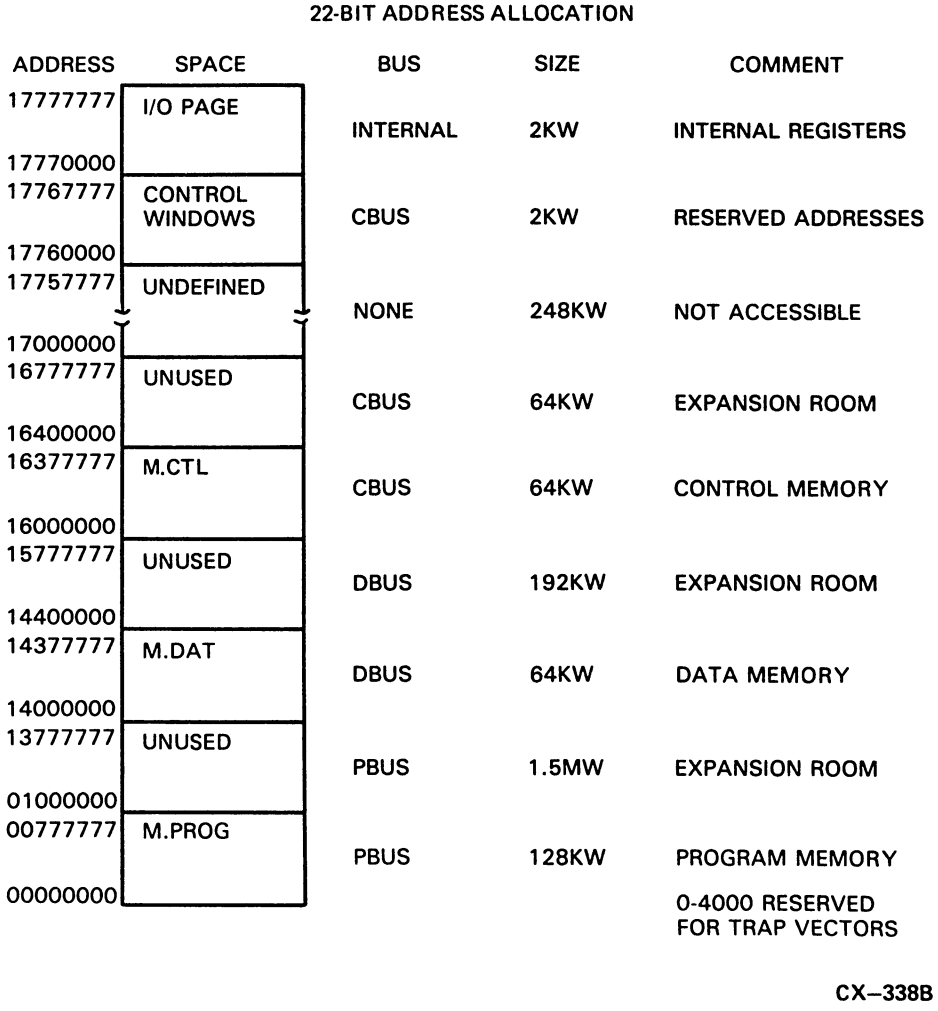
Commands and responses pass between the tape data channel microprocessor and other internal HSC50 processes through control memory. The tape data channel module interfaces to the control memory bus and to the data memory bus. Maximum configurations are outlined in the software release notes.

1.3.6 Memory Module (M.std) Functions

The memory module (L0106) contains the following three memories:

- 256 kbytes of program memory (M.prog) (space for the control program loaded from the TU58)
- 128 kbytes of control memory (M.ctl) (space for the routines initiating data transfer action)
- 128 kbytes of data memory (M.dat) (space to hold the data from/to a data channel module)

Using physical addresses, the memory space allocations for the three memories are illustrated in Figure 1-10.



22-BIT ADDRESS ALLOCATION

ADDRESS	SPACE	BUS	SIZE	COMMENT
17777777 17770000	I/O PAGE	INTERNAL	2KW	INTERNAL REGISTERS
17767777 17760000	CONTROL WINDOWS	CBUS	2KW	RESERVED ADDRESSES
17757777 17000000	UNDEFINED	NONE	248KW	NOT ACCESSIBLE
16777777 16400000	UNUSED	CBUS	64KW	EXPANSION ROOM
16377777 16000000	M.CTL	CBUS	64KW	CONTROL MEMORY
15777777 14400000	UNUSED	DBUS	192KW	EXPANSION ROOM
14377777 14000000	M.DAT	DBUS	64KW	DATA MEMORY
13777777 01000000	UNUSED	PBUS	1.5MW	EXPANSION ROOM
00777777 00000000	M.PROG	PBUS	128KW	PROGRAM MEMORY 0-4000 RESERVED FOR TRAP VECTORS

CX–338B

Figure 1-10 Memory Map (M.std – L0106)

Interface to control memory is by the backplane control bus and to data memory by the backplane data bus. The interface to the I/O control processor local program memory is via a set of backplane signals to the control memory module.

1.3.7 Input/Output (I/O) Control Processor Module (P.ioc) Functions

The I/O processor module (L0105) uses a PDP-11 ISP (F-11) processor with memory management and memory interfacing logic. This processor executes the HSC50 internal software. In addition, the I/O control processor module provides the following functions:

- Bootstrap read-only memory (ROM)
- Arbitration and control logic for the control and data buses
- Program-addressable registers for subsystem initialization and operator control panel communications

The I/O control processor module interfaces to:

- Program memory on the program memory bus
- Control memory through the signals of the backplane control bus
- Data memory through the signals of the backplane data bus
- TU58 tape drives
- Auxiliary terminal through an RS-232-C interface

More detailed information on the I/O processor is contained in Appendix A.

1.4 HSC50 MAINTENANCE STRATEGY

Maintenance of the HSC50 is accomplished with field replaceable units (FRUs). Procedures for removal and replacement are described in Chapter 3. Field service personnel should not attempt to replace or repair component parts within FRUs.

Isolation of solid failures can be accomplished efficiently due to the logical partitioning of the modules and extensive internal diagnostics. In addition to the device-resident diagnostics, the HSC50-resident confidence tests are available to support and verify corrective maintenance decisions.

1.5 MAINTENANCE FEATURES

The following features assist in troubleshooting the HSC50:

- Self-contained and self-initiated diagnostics
- Operator control panel fault code display
- Auxiliary terminal
- Module LED indicators

Various levels of diagnostics are executed in the HSC50. Read-only memory (ROM) diagnostics test each microprocessor in the disk and tape data channels, port processor, and input/output processor modules. All of the internal ROM diagnostics run by pressing the HSC50 Init button. This tests 95 percent of the HSC50.

Failures are displayed on the operator control panel or at the auxiliary terminal. If further diagnostics are needed, the auxiliary terminal can be used to initiate diagnostics stored on the TU58 tapes. (Refer to the *HSC50 Utilities User Documentation*, *Inline Diagnostics User Documentation*, and *Offline Diagnostics User Documentation*.)

Higher level diagnostics are loaded from the TU58 and run in the HSC50 to check SDI/STI communication and interaction between the HSC50 and disk or tape. Diagnostics are initiated on powerup, subsystem initialization or by operator command. All diagnostics necessary to troubleshoot the HSC50 are loaded through the TU58.

The HSC50 subsystem allows logical assignment of a disk drive or tape formatter to the diagnostics. Thus, drive diagnosis and repair is permitted although other drives connected to the HSC50 are active.

Background diagnostics test HSC50 logic not currently in use by the subsystem. Failures cause the HSC50 to reboot and execute the initialization diagnostics.

Detected data memory errors cause an initiation of the inline memory diagnostics to test the buffer causing the error. Failures found in any data buffer cause removal of that buffer from service. If no failure is found, the tested buffer is returned to service.

1.6 HSC50 SPECIFICATIONS

Figure 1-11 lists the HSC50 physical and environmental specifications.

1.7 HSC50 RELATED DOCUMENTATION

Documents related to the HSC50 are available under the following part numbers:

- *HSC50 User Guide*
  EK-HSC50-UG
- *HSC50 Installation Manual*
  EK-HSC50-IN
- *HSC50 Illustrated Parts Breakdown*
  EK-HSC50-IP
- *HSC50 Inline Diagnostics User Documentation*
  EK-IHSC5-UG
- *HSC50 Offline Diagnostics User Documentation*
  EK-OHSC5-UG
- *HSC50 Utilities User Documentation*
  EK-UHSC5-UG
- *DECwriter Correspondent Technical Manual*
  EK-CPL12-TM
- *TU58 DECtape II User Guide*
  EK-0TU58-UG
- *Star Coupler User Guide*
  EK-SC008-UG

These documents can be ordered from Publication and Circulation Services, 10 Forbes Road, Northboro, Massachusetts 01532 (RCS Code: NR12, Mail Code: NR03/W3).

DESCRIPTION	OPTION DESIGNATION
HSC50 MASS STORAGE SERVER	HSC50–AA = 60 HZ/120V
	HSC50–AB = 50 HZ/240V

MECHANICAL

MOUNTING CODE	WEIGHT		HEIGHT		WIDTH		DEPTH		CAB TYPE (IF USED)
	LBS	KG	IN	CM	IN	CM	IN	CM	
FS	400	181.2	42	106.7	21.3	54.1	36	91.4	MODIFIED H9642

POWER (AC)

AC VOLTAGE NOMINAL	AC VOLTAGE TOLERANCE	FREQUENCY & TOLERANCE	PHASE	STEADY–STATE CURRENT (RMS)	POWER CONSUMPTION (MAX)
120	104–128V	60 HZ ±1	3	13.5A	2228 WATTS
240	208–256V	50 HZ ±1	3	6.75A	2223 WATTS

POWER (AC)

AMPS (MAX) BY PHASE			
120V	0A = 0.7	240V	0A = 0.44
	0B = 14.2		0B = 7.09
	0C = 13.5		0C = 6.75

POWER (AC)

PLUG TYPE	POWER CORD LENGTH	INTERRUPT TOLERANCE	APPARENT POWER (KVA)
NEMA – L21 – 30P	15 FT (4 5 M)	4MS (MIN)	3.4 (KVA)

POWER (AC)

INRUSH CURRENT 60HZ	INRUSH CURRENT 50HZ	SURGE DURATION
65A RMS	130A RMS	1 CYCLE

DEVICE ENVIRONMENT

TEMPERATURE		RELATIVE HUMIDITY		RATE OF CHANGE		HEAT DISSIPATION	
OPERATING*	STORAGE	OPERATING	STORAGE	TEMP	HUMIDITY	BTU/HR	KJ/HR
50 – 104° F	–40 – 140° F	10 – 90%	10 – 90%	36° F/HR	20%/HR	7600	8021
10 – 40° C	–40 – +60° C			20° C/HR			

DEVICE ENVIRONMENT

ALTITUDE (MAX)		AIR VOLUME (AT INLET)		AIR QUALITY
OPERATING	STORAGE	FT^3 /MIN	DAL/MIN	PARTICLE COUNT (MAX)
8000 FT	30,000 FT	210	75.6	N/A
2.4 KM	9.1 KM			

* ALTITUDE CHANGES: DE-RATE THE MAXIMUM TEMPERATURE 1.8° C PER THOUSAND METERS (1.0° F PER THOUSAND FEET).

CX–280A

Figure 1-11 HSC50 Specifications

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CHAPTER 2
HSC50 CONTROLS/INDICATORS

2.1 INTRODUCTION

This chapter describes the controls and indicators located in five areas of the HSC50:

- Operator Control Panel (OCP)
- Inside the front door
- Maintenance access panel
- Logic modules
- Power controllers (60 Hz and 50 Hz)

2.2 OPERATOR CONTROL PANEL

Figure 2-1 illustrates the controls and indicators on the operator control panel.

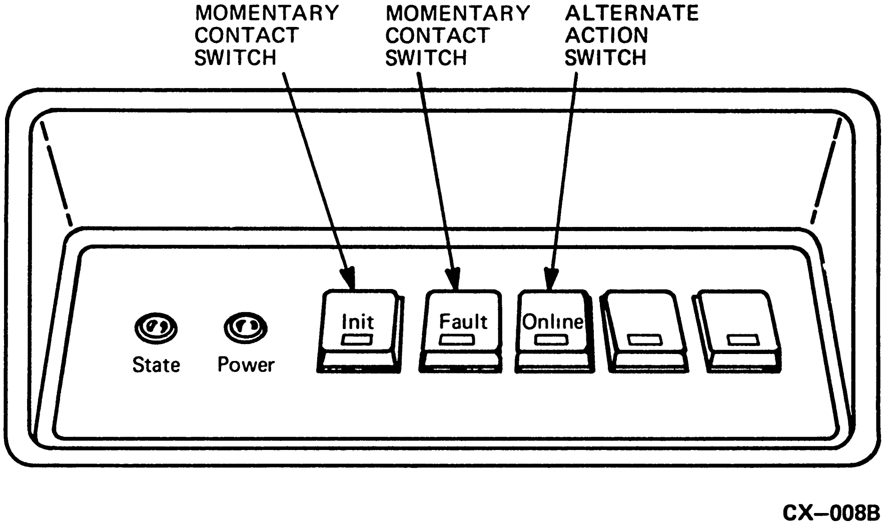


Figure 2-1 Operator Control Panel

2.2.1 State and Init Indicators

These indicators describe the state of the HSC50. Under runtime conditions, the Init indicator is off while the State indicator is pulsing. During initialization, these indicators change to reflect the current initialization phase of the subsystem. Refer to the bootstrap flowchart in Chapter 5 for details on these phases.

2.2.2 Init Switch

Pushing the Init switch causes the HSC50 to start its initialization routine. The Secure/Enable switch must be in the ENABLE position for this switch to be operational.

2.2.3 Power Indicator

Also located on the Operator Control Panel is the Power indicator. The Power indicator is driven from a dc comparator circuit on the I/O Control Processor module (L0105). This circuit constantly monitors the +5, +12, and −5.2 voltages. If it detects a drop of approximately one-third in any of these three voltages, the indicator goes off. Note, the Power indicator being on does not mean these voltages are within specification (plus or minus 5 percent).

2.2.4 Fault Indicator and Switch

The Fault indicator comes on when the HSC50 logic detects a fault. The Fault switch is used for the OCP lamp test.

2.2.4.1 Fault Codes – When the Fault switch is pressed and released, the lamps in Init, Online, Fault, and the two blanks function as an error display. The fault code blinks on and off until the HSC50 is powered down or the Init switch pressed again. Error codes associated with the OCP display are defined in Chapter 5.

2.2.4.2 Lamp Test – Pushing and holding the Fault switch causes all the OCP indicators to light and function as a lamp test. These indicators go off when the switch is released. Even if the Fault indicator is already on before the switch is pushed, the lamp test can be executed.

2.2.5 Online Switch

When the Online switch is pushed to the in position, the HSC50 logic is put in the available state. This allows a host to establish a virtual circuit with the HSC50. When this switch is released to the out position, no new virtual circuits can be made and the indicator goes off when the last virtual circuit is broken. The HSC50 is then in an offline state (Online switch out and Online indicator off).

2.2.6 Online Indicator

When the Online indicator is on, a virtual circuit is established between the HSC50 and a host CPU. When this indicator is off, no virtual circuits are established with any host.

2.2.7 Blank Indicators

The two blank indicators form a part of the fault display to produce a 5-bit fault code.

2.3 INSIDE FRONT DOOR CONTROLS/INDICATORS

Figure 2-2 shows the controls and indicators available when the front door is opened.

2.3.1 Secure/Enable Switch

With the Secure/Enable switch in the SECURE position, the Init switch is disabled from the OCP. Also, the SET utility program cannot run and the BREAK character from the terminal is disabled. With the Secure/Enable switch in the ENABLE position, the Init switch and all the utility programs can be used. The SHOW utility is operable with the Secure/Enable switch in either position.

2.3.2 Enable Indicator

An illuminated Enable LED indicates the Secure/Enable switch is in the ENABLE position (all switches can be used). When the Enable indicator is off, the OCP is secure.

2.3.3 TU58 Run Indicators

When a TU58 Run indicator is on, the TU58 is currently moving tape. Data loss can occur if the tape is removed while this indicator is on. If the indicator is off, tape is not in motion.

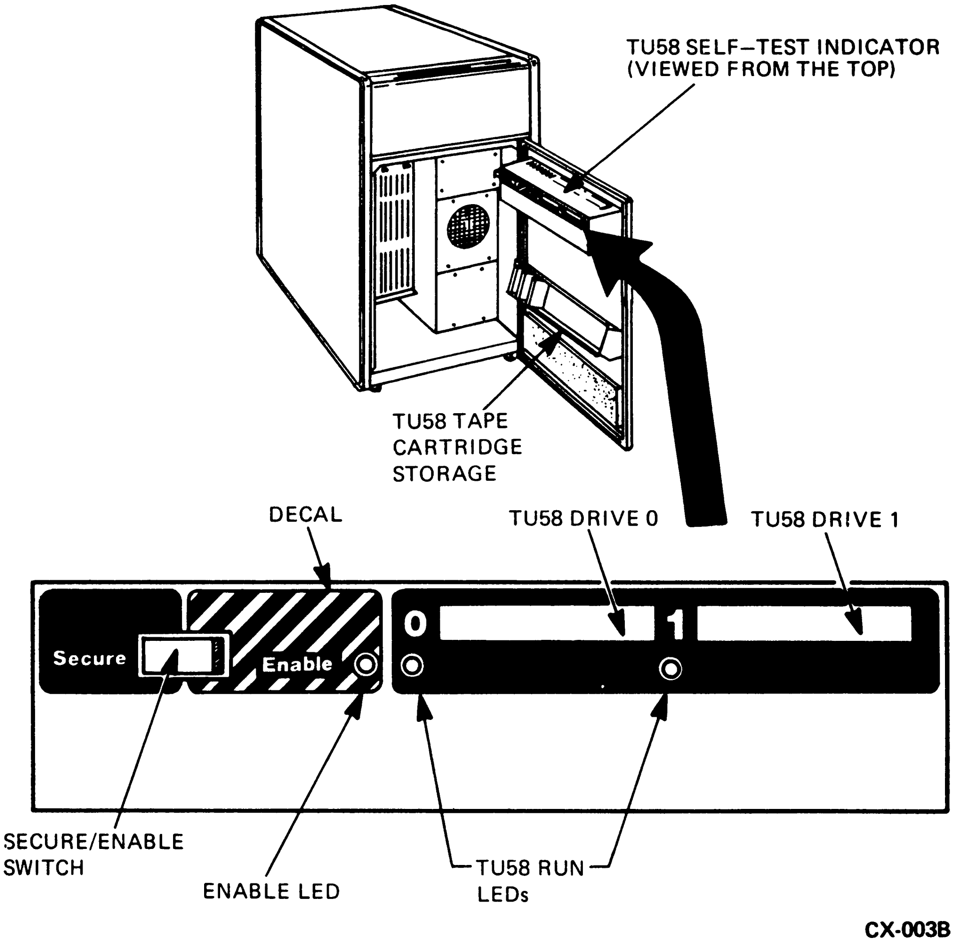


Figure 2-2 Controls/Indicators – Inside Front Door

2.3.4 TU58 Self-Test Indicator

The TU58 Self-Test indicator is found on the TU58 controller module (Figure 2-2). The controller module is located inside the TU58 housing with the drive mechanics. Observe the Self-Test indicator by looking down through the TU58 housing vents. When this indicator is on, the TU58 controller has successfully completed self-diagnostics.

2.4 MAINTENANCE ACCESS PANEL CONTROLS AND CONNECTORS

Removing the maintenance access panel cover reveals the DC Power switch and several connectors available for HSC50 maintenance. (Refer to Figure 2-3.) Voltage test points on this panel are illustrated in Chapter 5.

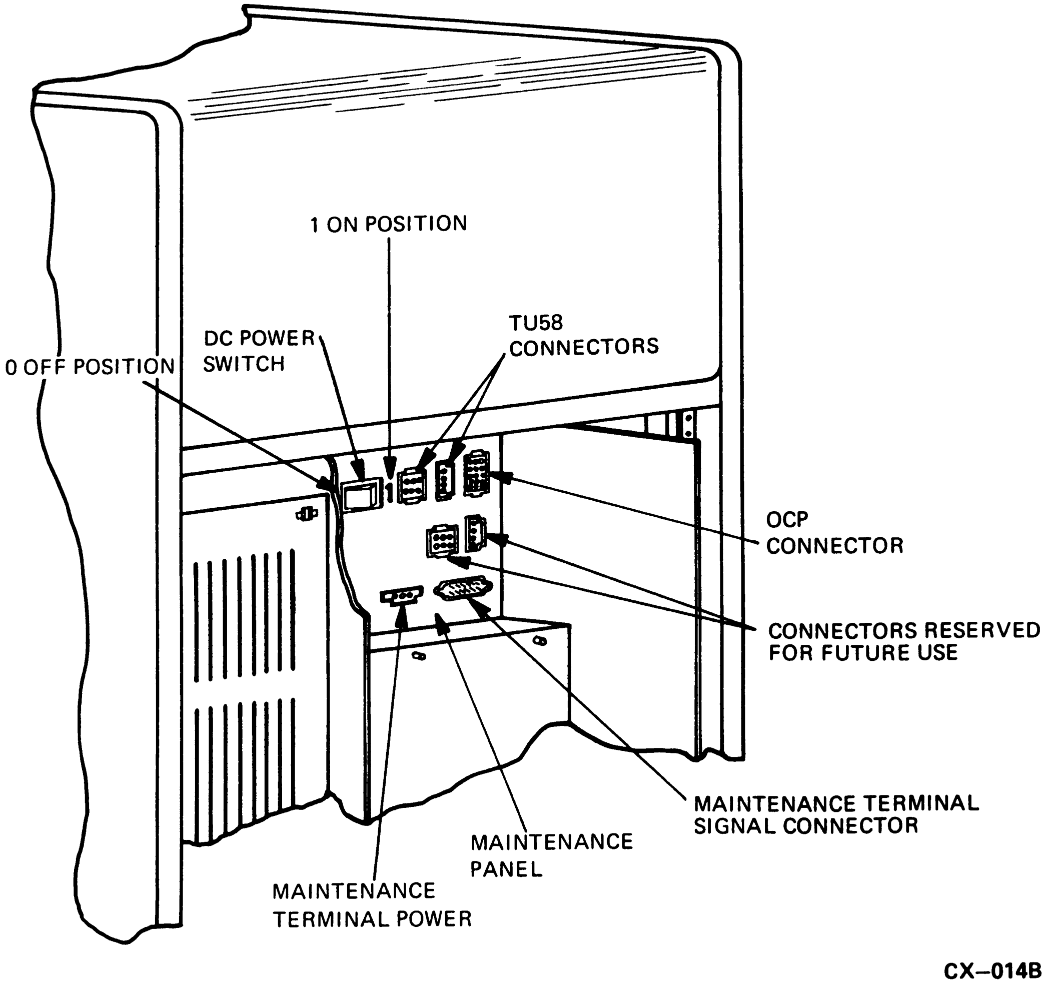

1 ON POSITION
DC POWER SWITCH
TU58 CONNECTORS
0 OFF POSITION
OCP CONNECTOR
CONNECTORS RESERVED FOR FUTURE USE
MAINTENANCE TERMINAL SIGNAL CONNECTOR
MAINTENANCE PANEL
MAINTENANCE TERMINAL POWER
CX–014B

Figure 2-3 Maintenance Access Panel

2.4.1 DC Power Switch

When the DC Power switch is in the "0" position, the HSC50 is without dc power. Moving the switch to the "1" position restores dc power.

2.4.2 Maintenance Panel Connectors

Two of the connectors in the maintenance access panel are used to connect the maintenance terminal to the HSC50. One connector supplies power to the maintenance terminal and the other is the signal connector. Additional connectors are:

- OCP connector
- TU58 connector
- Connectors reserved for future use

2.5 MODULE INDICATORS AND SWITCHES

All logic modules have at least one LED to indicate board status. Refer to Figure 2-4 for the locations of these LEDs. Additionally, three of these logic modules contain specific switches or fuses.

Figure 1-4 shows the slot location for each of the modules.

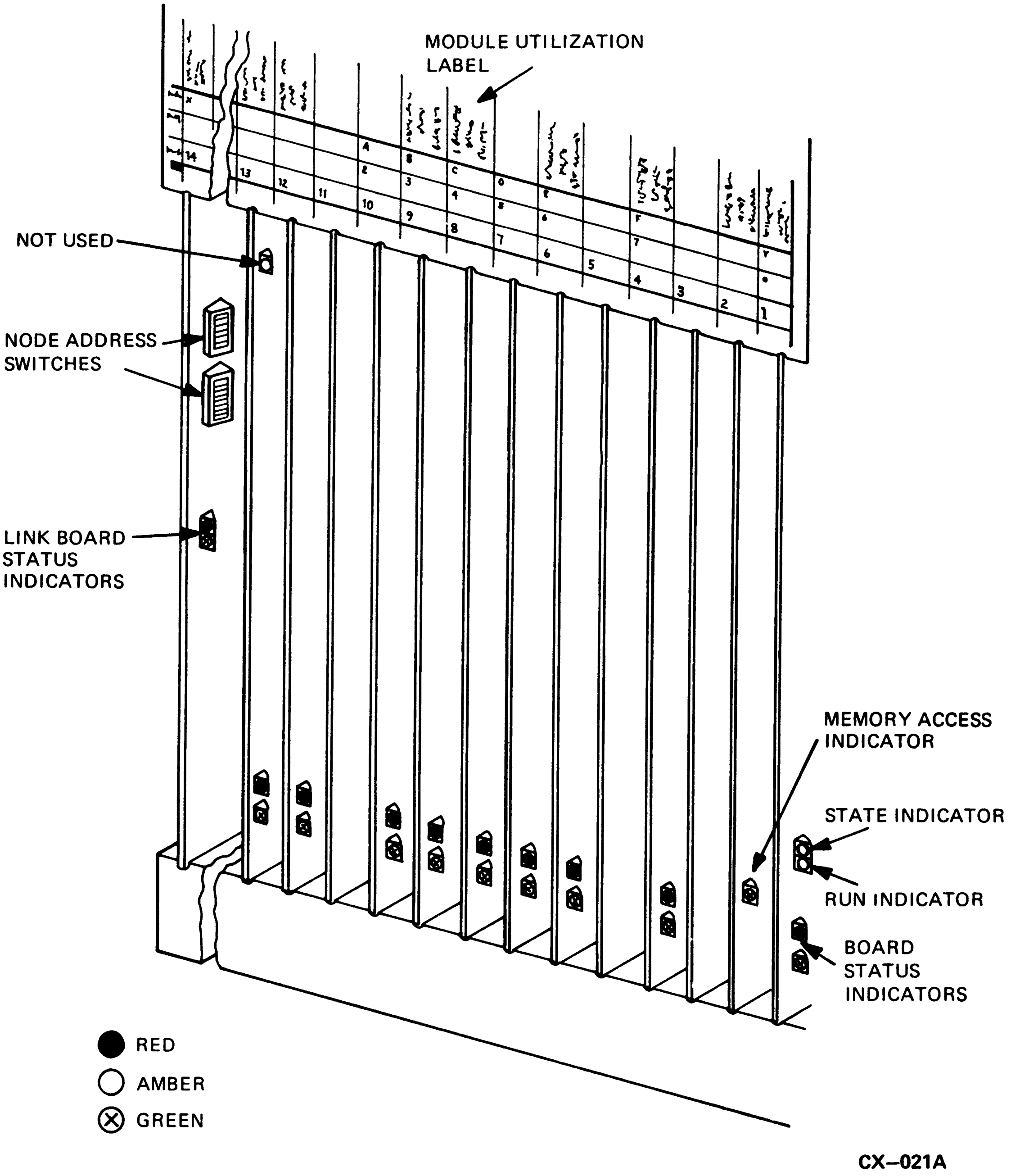


Figure 2-4 Module LED Indicators

2.5.1 Module Indicators

Refer to Table 2-1 for the functions of the various module LEDS.

Table 2-1 Functions of Logic Module LEDs

Module	Color	Function
L0105, L0108-YA, L0108-YB, L0107-YA, 10109	Green	Indicates the operating software is running.
L0105, L0108-YA, L0108-YB, L0107-YA, L0109	Red	Indicates an inoperable module except during initialization when it comes on during module testing.
L0106	Green	Indicates memory cycles are operating.
L0105	Amber	Top one mirrors the OCP State indicator. Second one pulses at the on-board microprocessor run rate.
L0100	Green	Indicates the node is either transmitting or receiving. Dims or brightens relative to the amount of local CI activity.
L0100	Red	Indicates the module is in the Internal Maintenance mode.
L0109	Amber	Always on when the HSC50 is online. (Used only for engineering debug test purposes.)

2.5.2 Module Switches

Specific switches are found on L0100, L0105, L0107, and L0109, as follows.

2.5.2.1 Port Link Module (L0100) – Figure 2-4 shows the location of the CI node address switches mounted on the L0100 module. Both sets of switches must be identically set to avoid CI addressing errors. The chosen address must not exceed the current maximum of 15 (decimal). Addresses higher than 15 cause Port Link module faults on the OCP (error code of 25 octal).

2.5.3 I/O Control Module (L0105)

The L0105 module contains a baud rate jumper (W3) to establish the proper communication rate between the HSC50 and its attached auxiliary terminal. Figure 2-5 shows the location of the jumper controlling baud rate, either:

Jumper W3 in = 9600 baud
or
Jumper W3 out = 300 baud

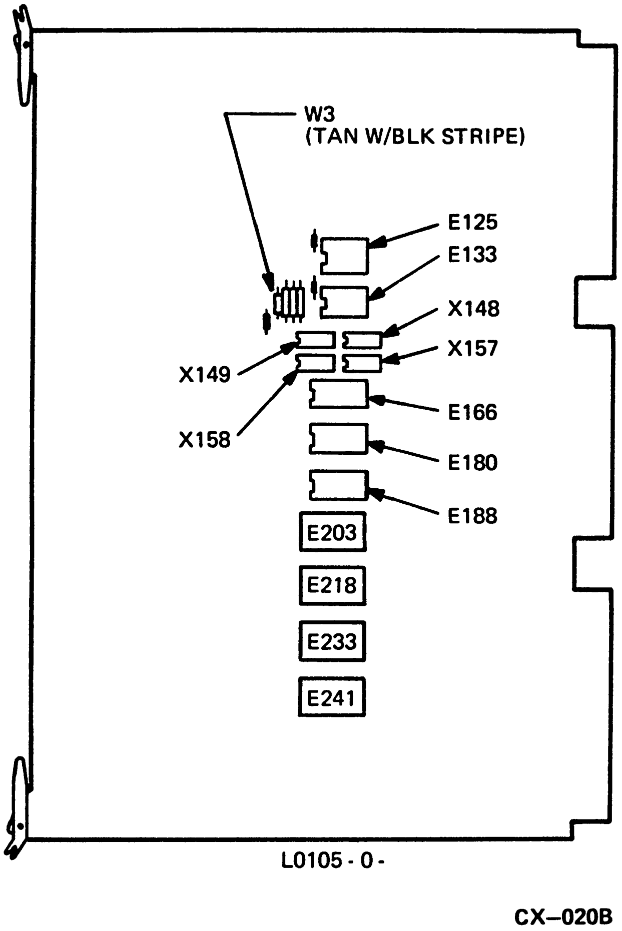


Figure 2-5 Baud Rate Jumper

2.5.4 Port Link and Port Link Buffer Modules (L0107 and L0109)

Both the L0107 and L0109 modules have Dual Inline Pack (DIP) switches to indicate the hardware revision level. DIP switch positions should not be changed except as directed by a Field Change Order. Figure 2-6 shows the location of the these switches.

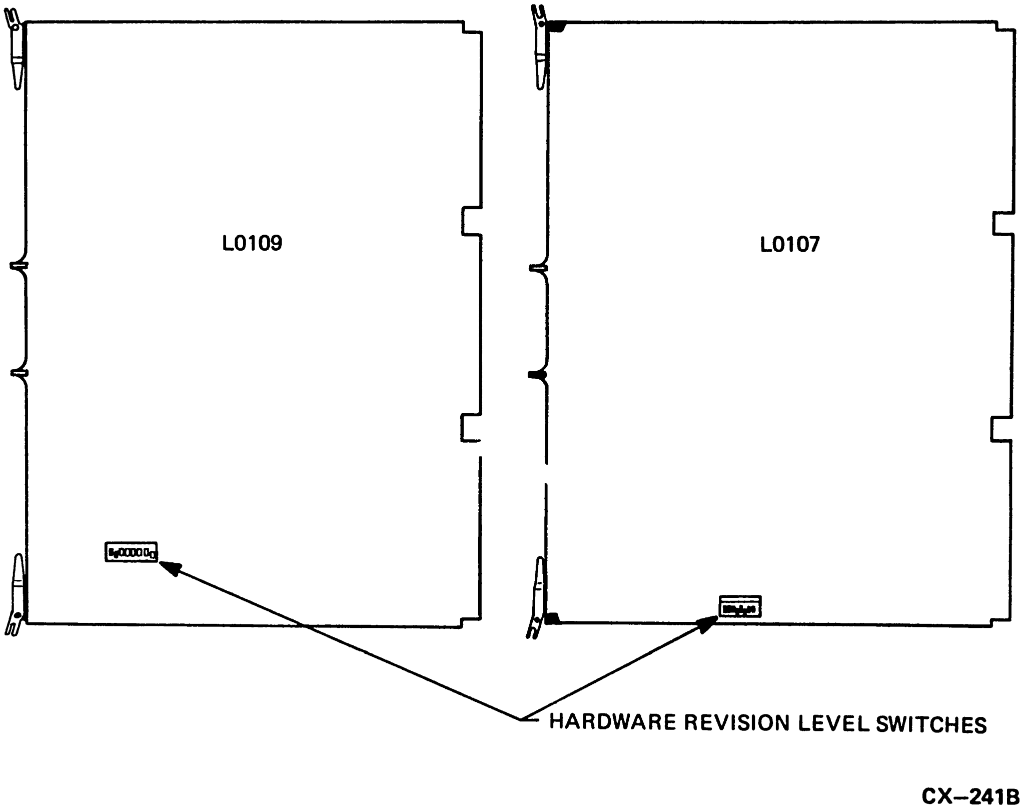
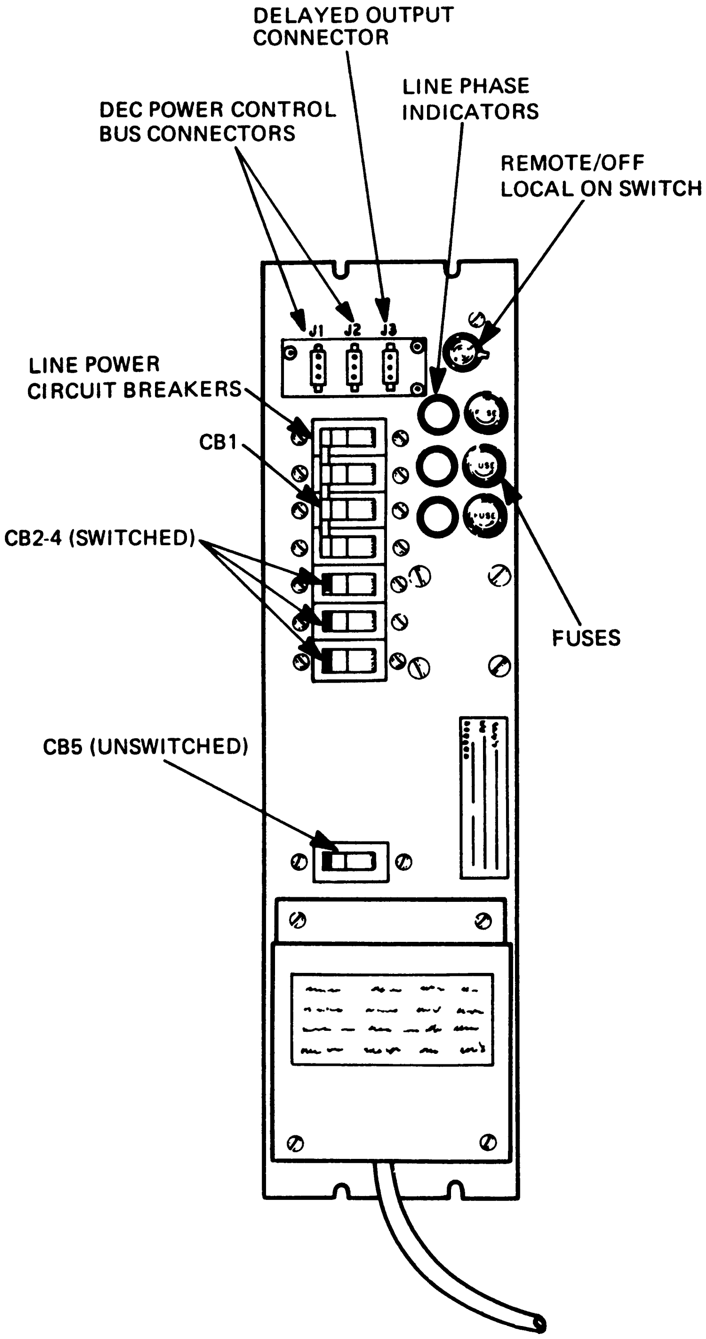


Figure 2-6 Module (ID) S/N Switches

2.6 POWER CONTROLLER

The 60 Hz power controller is shown in Figures 2-7 and 2-9. For the 50 Hz unit, refer to Figures 2-8 and 2-10. A physical description of the power controller follows.



CX–013B

Figure 2-7 Power Controller (60 Hz) – Front View

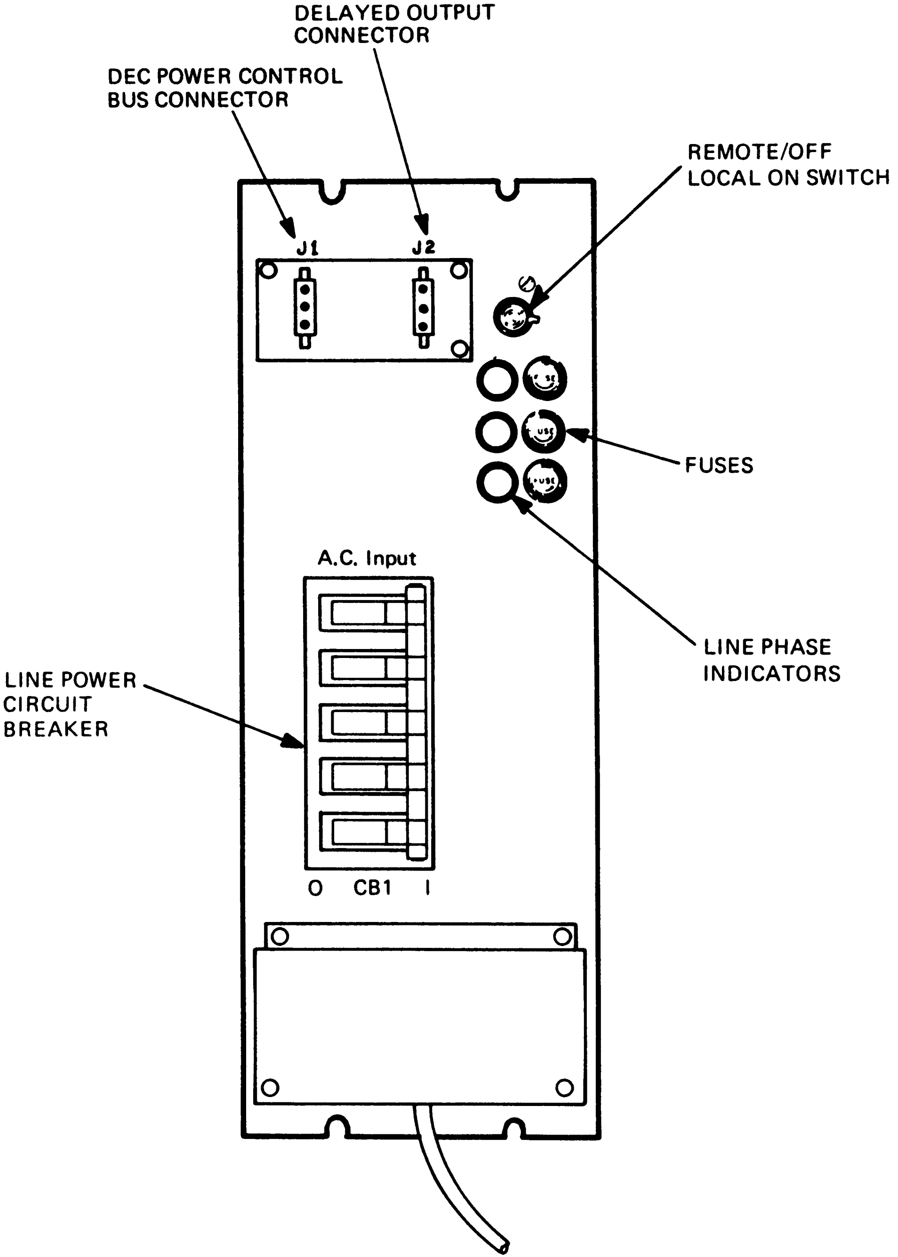

DELAYED OUTPUT CONNECTOR
DEC POWER CONTROL BUS CONNECTOR
REMOTE/OFF LOCAL ON SWITCH
J1
J2
FUSES
A.C. Input
LINE PHASE INDICATORS
LINE POWER CIRCUIT BREAKER
O
CB1
I
CX–013C

Figure 2-8 Power Controller (50 Hz) – Front View

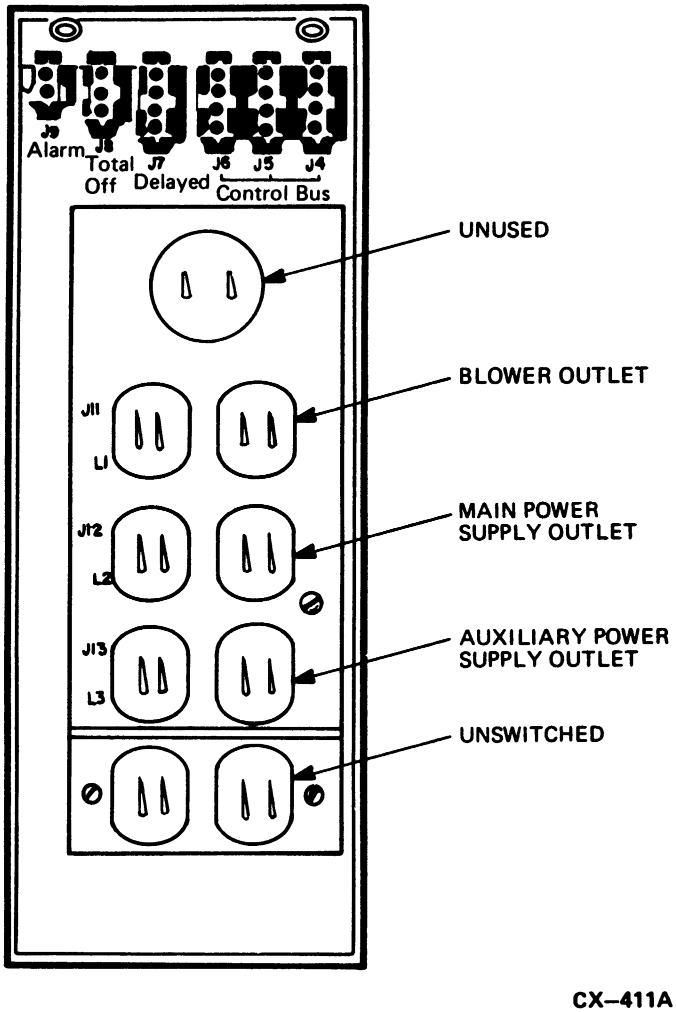


Figure 2-9 Power Controller (60 Hz) – Rear View

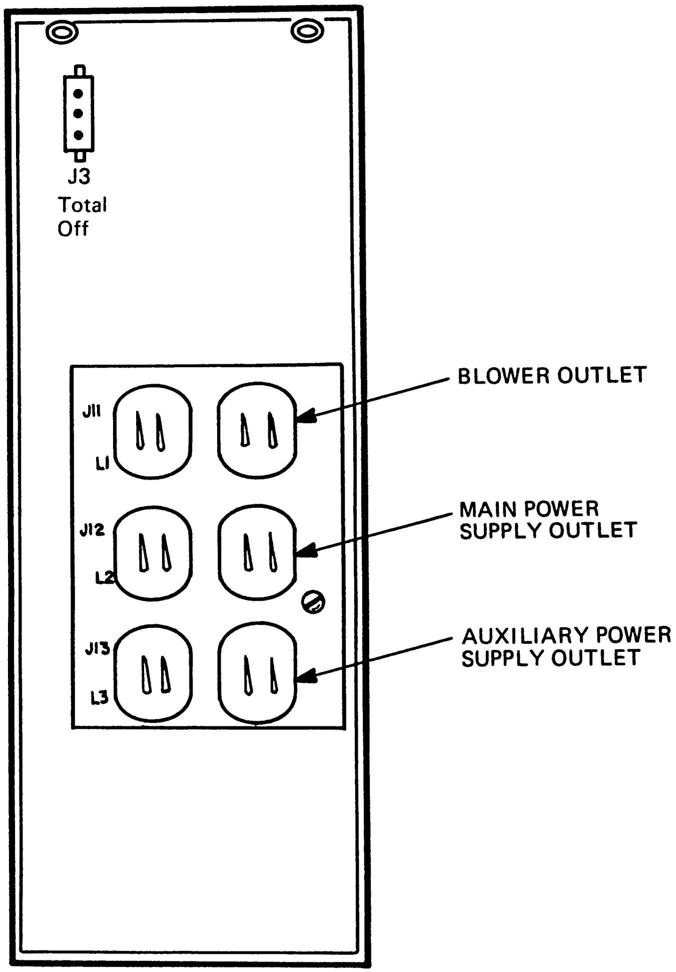


Figure 2-10 Power Controller (50 Hz) – Rear View

2.6.1 Line Phase Indicators

Three Line Phase indicators display the status of incoming line power. If any phase drops, the indicator for that phase goes off.

2.6.2 Fuses

The three line phases are fused to protect the HSC50 circuitry. These fuses are located beside the Line Phase indicators.

2.6.3 Remote/Off/Local On Switch

When this switch is in the off position, the power controller does not route ac line power to the switched or unswitched outlets.

With the switch in the local on position, ac power is routed to the power controller switched or unswitched outlets.

When the switch is in the remote position, the routing of ac power is dependent upon the power control bus signals.

2.6.4 Circuit Breakers (60 Hz)
Five power controller circuit breakers perform the following functions:

- CB1 – Protects from incoming power surges.
- CB2-4 – Protect the switched outlets (Figure 2-7).
- CB5 – Protects the unswitched outlets.

2.6.5 Circuit Breakers (50 Hz)
The 50 Hz unit contains one circuit breaker (Figure 2-8). CB1 on this unit protects all circuits.

2.6.6 Power Controller (60 Hz) – Rear View
The switched outlets in Figure 2-9 are protected by CB2-4 (Figure 2-7) and the bottom (unswitched) by CB5. Both the bottom and top outlets are currently unused.

J8 at the top of the power controller (rear), labeled Total Off, connects the air flow sensor.

2.6.7 Power Controller (50 Hz) – Rear View
Outlets in Figure 2-10 are protected by CB1 (Figure 2-8). J3, shown at the top of the 50 Hz power controller rear view (Figure 2-10) connects the air flow sensor.

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CHAPTER 3
REMOVAL AND REPLACEMENT PROCEDURES

3.1 INTRODUCTION

This chapter describes procedures for removing and replacing the field replaceable units (FRUs) in an HSC50. Section 3.4 shows the proper sequence for FRU removal.

3.2 SAFETY PRECAUTIONS

Because hazardous voltages exist inside the HSC50, only a qualified service representative should service the subsystem. Bodily injury or equipment damage can result from improper servicing.

WARNING

Always remove power from the HSC50 before replacing internal parts or cables.

3.3 REMOVING POWER

Before removing/replacing a FRU, turn off the ac power. Open the back door with 5/32-inch hex wrench (Figure 1-5). The power controller is located on the lower left side of the cabinet. Figures 2-7 and 2-8 show the location of the circuit breakers on the 60 Hz and 50 Hz units, respectively.

3.3.1 Removing AC Power

To remove ac power, turn off CB1 (Figures 2-7 and 2-8).

3.3.2 Removing DC Power

Following are the three methods for removing dc power:

- Turning off the dc power switch, located on the maintenance access panel (Figure 2-3).
- Turning off CB1 (ac power).
- Turning the 3-position Remote/Off Local On switch to the OFF position (Figures 2-7 and 2-8).

3.4 REMOVAL SEQUENCE

Figure 3-1 shows the FRU removal sequence for an HSC50. Numbers shown in parentheses indicate the paragraph location for each procedure.

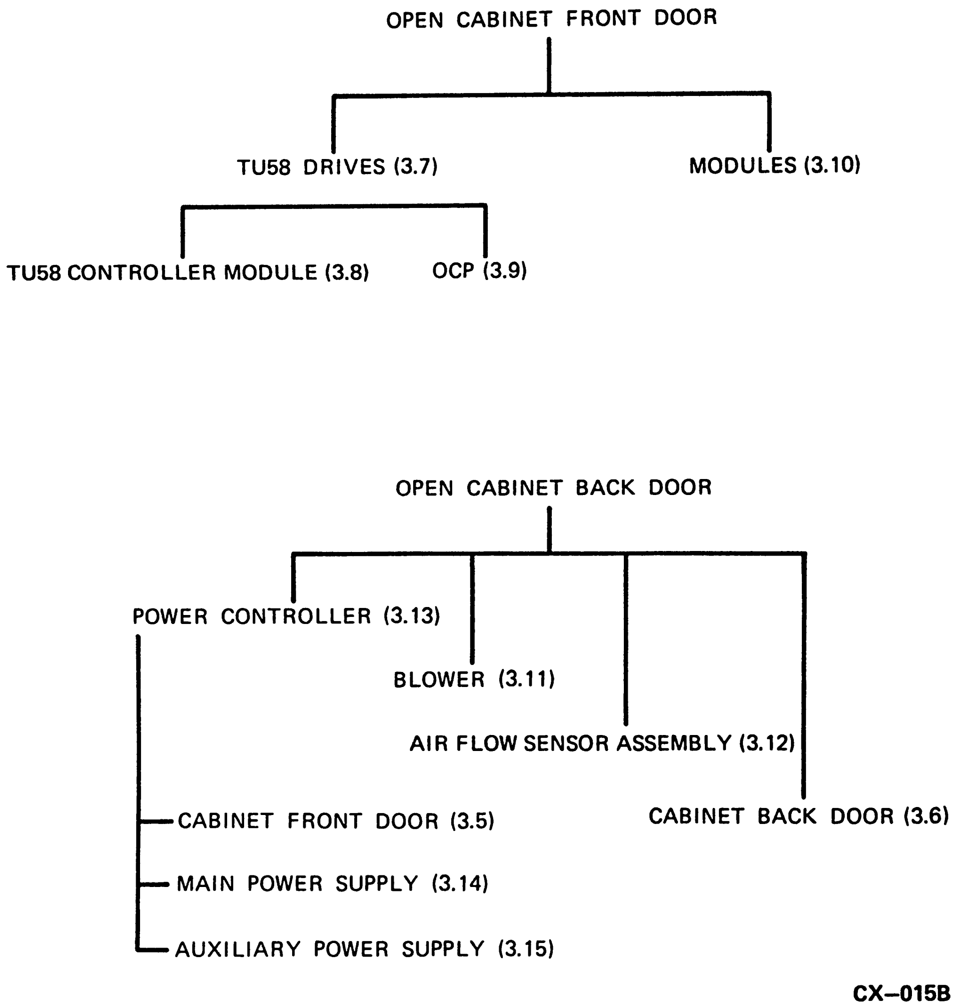


Figure 3-1 FRU Removal Sequence

3.5 CABINET FRONT DOOR

1. Open the cabinet front door by turning the key clockwise.

CAUTION
When performing the following steps, take care not to damage the front spring fingers.

2. Disconnect the ground wire from the door.
3. Remove the maintenance access panel by loosening the four captive screws.

NOTE
Some HSC50s have a hinged maintenance access panel with only one captive screw.

4. Remove HSC50 power by pushing the dc power switch to the "0" position.
5. Remove the plastic cable duct cover.

6. Disconnect cables from the maintenance access panel (Figure 2-3).
7. Pull down on the spring-loaded rod on the top hinge inside the cabinet and then lift the door off its bottom pin.
8. Reverse the removal procedure to replace the front door.

3.6 CABINET BACK DOOR

1. Open the back door with a 5/32-inch hex wrench.
2. Pull down on the spring-loaded rod on the top hinge inside the cabinet and then lift the door off its bottom pin.
3. Reverse the removal procedure to replace the back door.

3.7 TU58 BEZEL ASSEMBLY

1. Open the front door.
2. Remove the maintenance access panel by loosening the four captive screws.
3. Remove HSC50 dc power by pushing the dc power switch to the "0" position.
4. Remove the two locknuts on the bottom of the TU58 bezel assembly (Figure 3-2).

CAUTION
When servicing the TU58, avoid bending the tachometer disk mounted on the drive motor shaft. If the disk is bent, but not creased, it may be straightened. If it cannot be straightened or if it is creased, the TU58 must be replaced. The disk should not rub against the optical sensor block or any dangling wires.

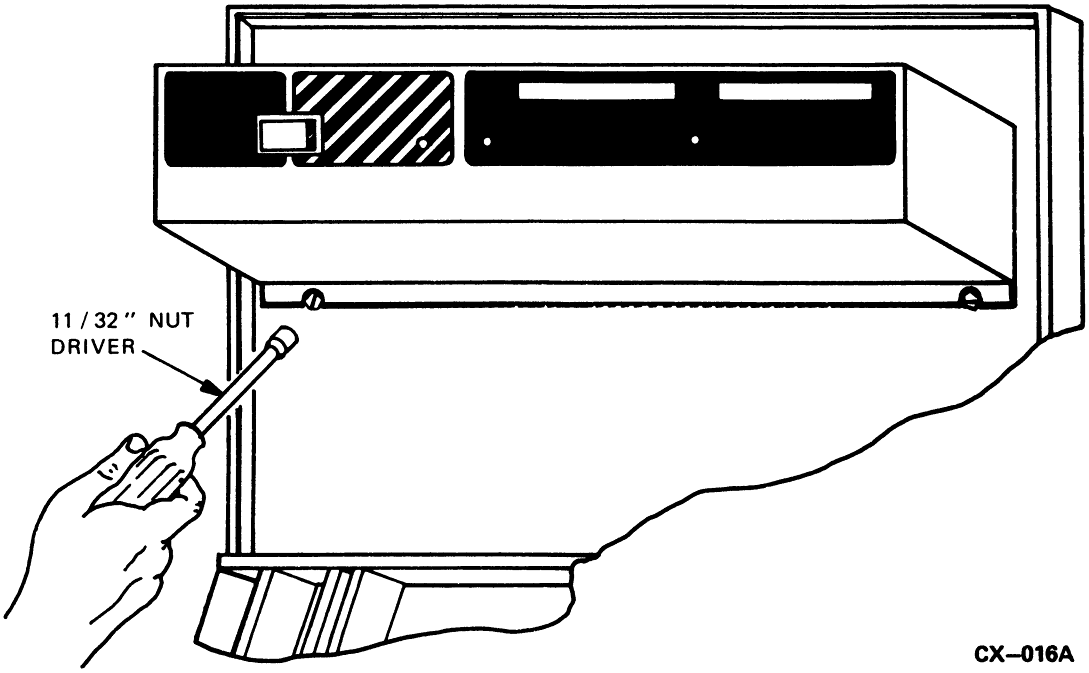


Figure 3-2 TU58 Bezel Assembly Removal

5. Push the TU58 bezel assembly up about an inch to clear the mounting hooks from their slots. Pull the bezel assembly back three to four inches from the door for clearance.
6. Support the TU58 bezel assembly with one hand while disconnecting J3 and J4 from the OCP (Figure 3-3).
7. Disconnect cables from the TU58 controller module (Figure 3-4).

NOTE
The head cover shown upper left in Figure 3-4 should be removed during operation.

8. Slide the controller module out of the plastic guides.
9. Reverse the removal procedure to replace the TU58 drives.

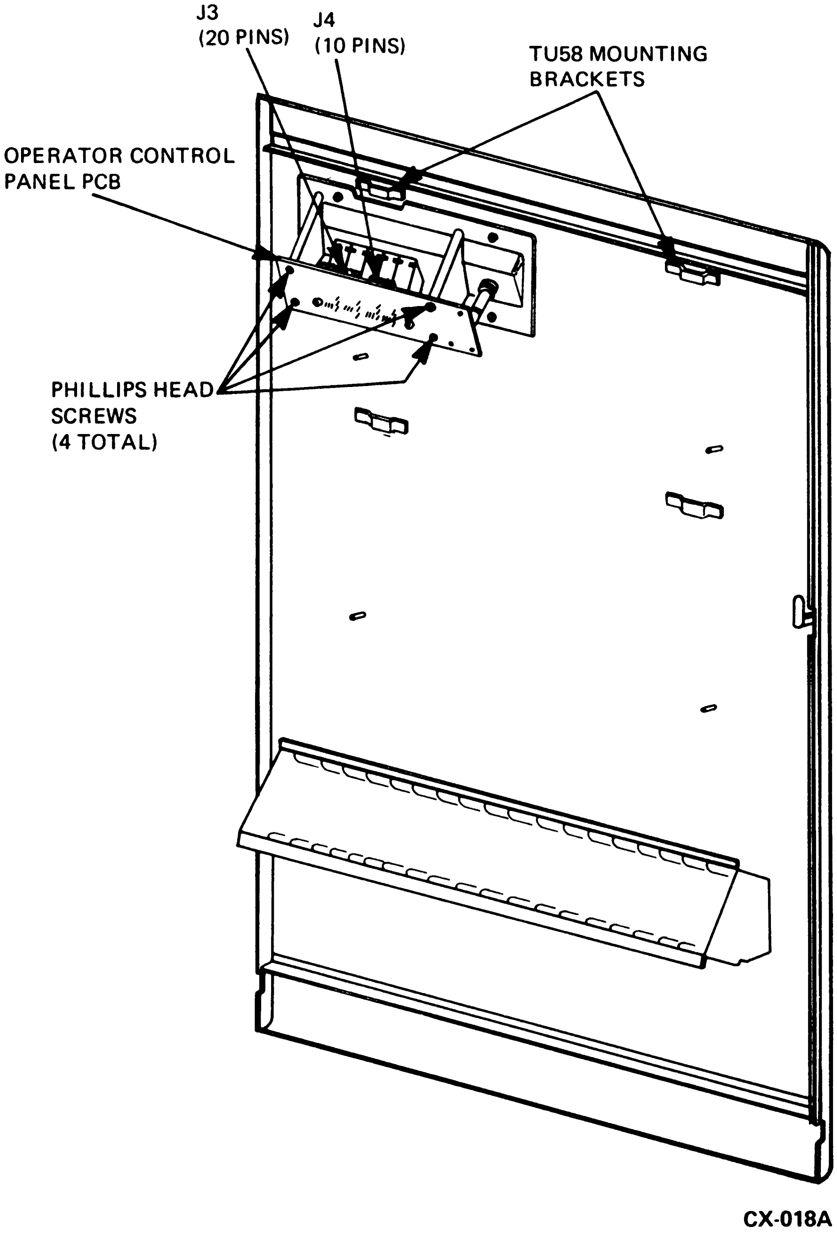


Figure 3-3 Operator Control Panel Removal

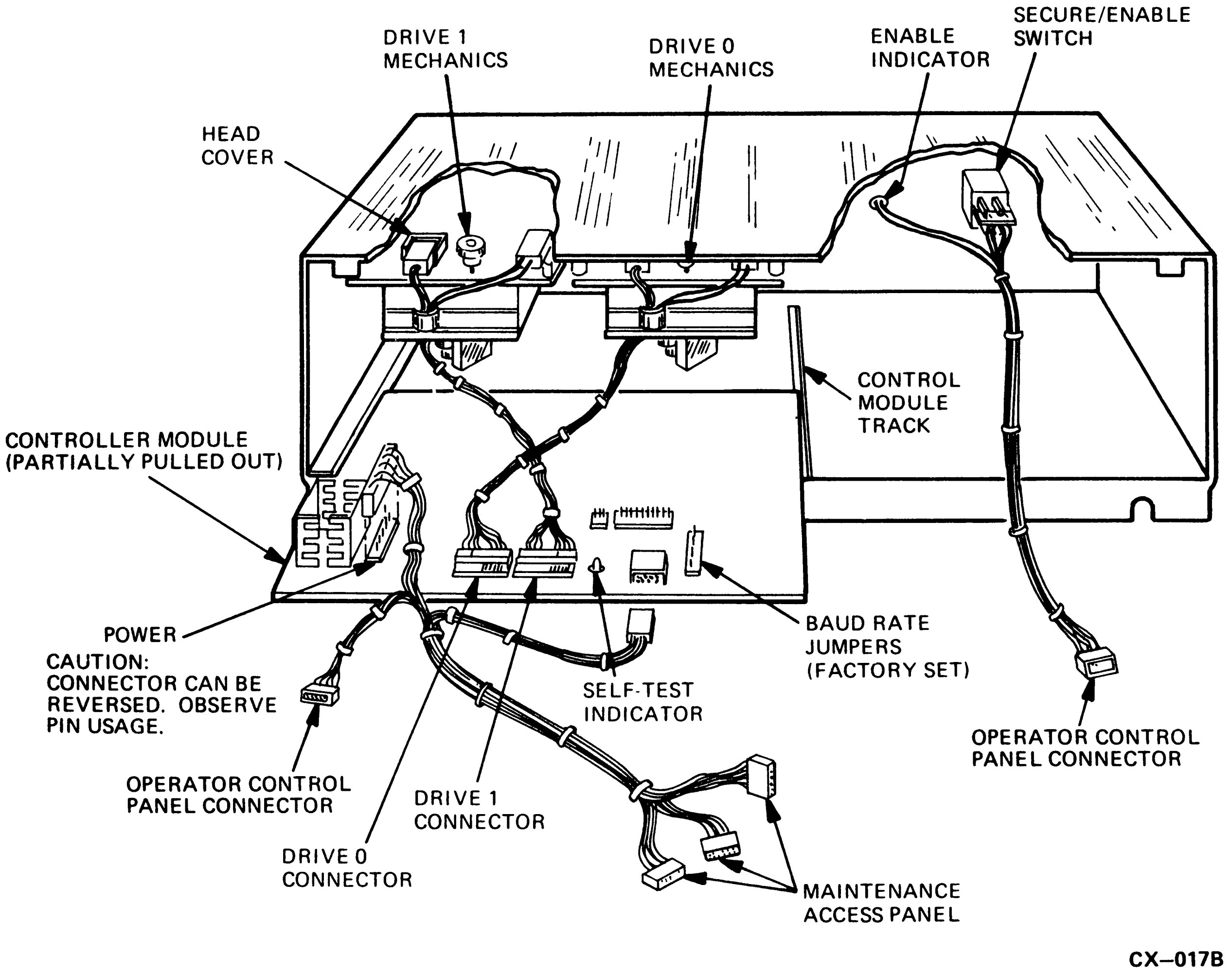

DRIVE 1 MECHANICS
DRIVE 0 MECHANICS
ENABLE INDICATOR
SECURE/ENABLE SWITCH
HEAD COVER
CONTROL MODULE TRACK
CONTROLLER MODULE (PARTIALLY PULLED OUT)
POWER
CAUTION: CONNECTOR CAN BE REVERSED. OBSERVE PIN USAGE.
BAUD RATE JUMPERS (FACTORY SET)
SELF-TEST INDICATOR
OPERATOR CONTROL PANEL CONNECTOR
OPERATOR CONTROL PANEL CONNECTOR
DRIVE 1 CONNECTOR
DRIVE 0 CONNECTOR
MAINTENANCE ACCESS PANEL
CX–017B

Figure 3-4 TU58 Controller Removal

3.8 TU58 CONTROLLER MODULE

1. Perform steps 1 through 8 of the TU58 drives removal procedure.
2. Ensure the baud rate jumper setting on the new module is the same as on the replaced module. Refer to Figure 3-4 for jumper location.
3. Reverse the removal procedure to replace the TU58 controller module.

3.9 OPERATOR CONTROL PANEL

OCP indicators are not field replaceable. If any lamp fails, replace the entire OCP as follows:

1. Open the front door by turning the key clockwise.
2. Remove dc power.
3. Remove TU58s (paragraph 3.7)
4. Remove J3 and J4 from the OCP (Figure 3-3).
5. Remove the four screws from the OCP (Figure 3-3).
6. Carefully pull out the OCP, allowing for indicator and switch clearance.
7. Reverse the removal procedure to replace the OCP.

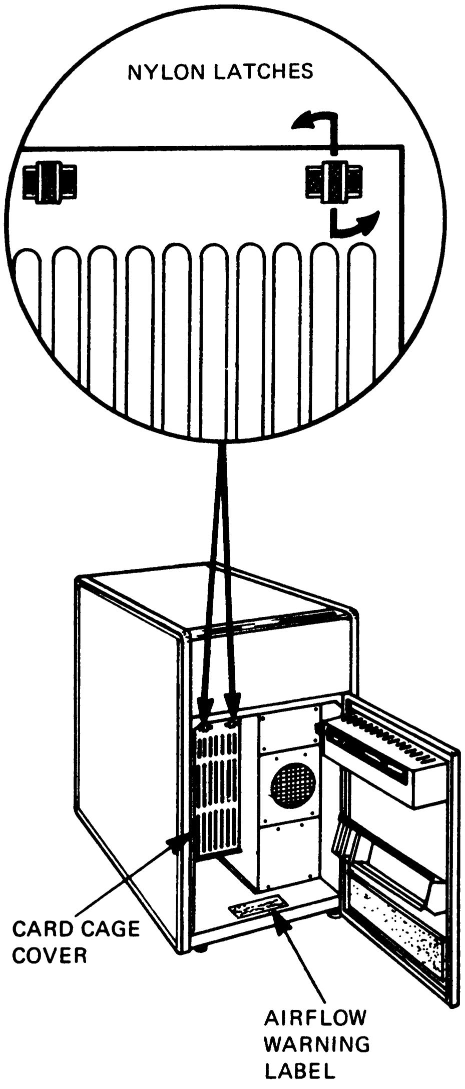
3.10 LOGIC MODULES

A Velostat (antistatic) kit must be used during module removal/replacement. The Velostat kit part number is 29-11762.

1. Open the front door by turning the key clockwise.
2. Remove dc power.
    - Open the maintenance access panel.
    - Push the DC Power switch to the "0" position (off).
3. Turn the two nylon latches on the module cover plate one-quarter turn (Figure 3-5).
4. Pull the card cage cover up and out.
5. Check the module utilization label above the card cage for the location of the desired module. The module slots are numbered from right to left, viewed from the module cover side.
6. Remove the module and replace with a new one.
7. Reverse the removal procedure to replace the card cage cover.

NOTES

- **The I/O control processor module is identified by factory-set jumpers. Each module has a unique serial number that matches the pattern of the jumpers. Do not reconfigure these jumpers.**
- **If an I/O control processor module is being replaced, set the baud rate jumper to match the terminal in use (Figure 2-5). To set the baud rate for 9600, leave jumper W3 intact. To set a baud rate of 300, cut one elbow angle on the W3 lead and spread slightly to avoid contact between the cut edges.**
- **If the Port Link module is being replaced, ensure the node address switches are properly set on the new module. Figure 2-4 shows the location of the switches. See the system manager for the correct node address.**



CX–019A

Figure 3-5 Card Cage Cover Removal

3.11 BLOWER

1. Open the back door using a 5/32-inch hex wrench.
2. Turn off ac power (CB1 on the power controller).
3. Disconnect the blower power connector.
4. Remove the exhaust duct from the bottom of the blower by lifting up the quick release latches on each side of the duct (Figure 3-6).
5. Loosen, but do not remove, the three Phillips screws holding the blower mounting bracket to the cabinet.
6. Lift the blower and bracket up and out of the cabinet.
7. Reverse the removal procedure to replace the cooling blower.

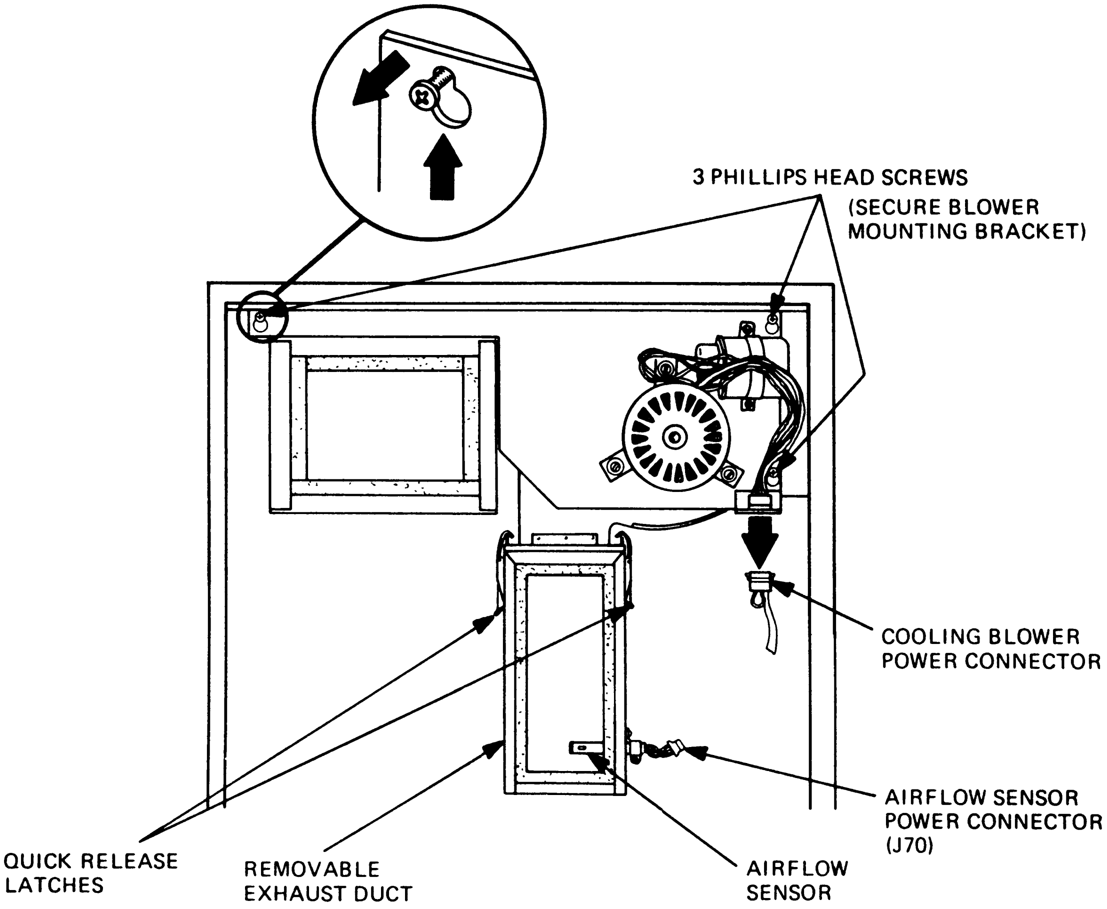

3 PHILLIPS HEAD SCREWS
(SECURE BLOWER MOUNTING BRACKET)
COOLING BLOWER POWER CONNECTOR
AIRFLOW SENSOR POWER CONNECTOR (J70)
QUICK RELEASE LATCHES
REMOVABLE EXHAUST DUCT
AIRFLOW SENSOR
CX–046A

Figure 3-6 Main Cooling Blower Removal

3.12 AIRFLOW SENSOR ASSEMBLY

1. Open the back door using a hex wrench.
2. Turn off the ac circuit breaker (CB1) on the HSC50 power controller.
3. Disconnect J70 (Figure 3-7).
4. Remove Phillips head screw that holds mounting clamp to the duct.
5. Slide sensor assembly out of duct.
6. Reverse the removal procedure to replace the airflow sensor assembly.
7. Align the slots in the airflow sensor tip horizontally with the floor.
8. Ensure sensor operability by blocking the flow of air. Pinching the sensor should trip CB1.

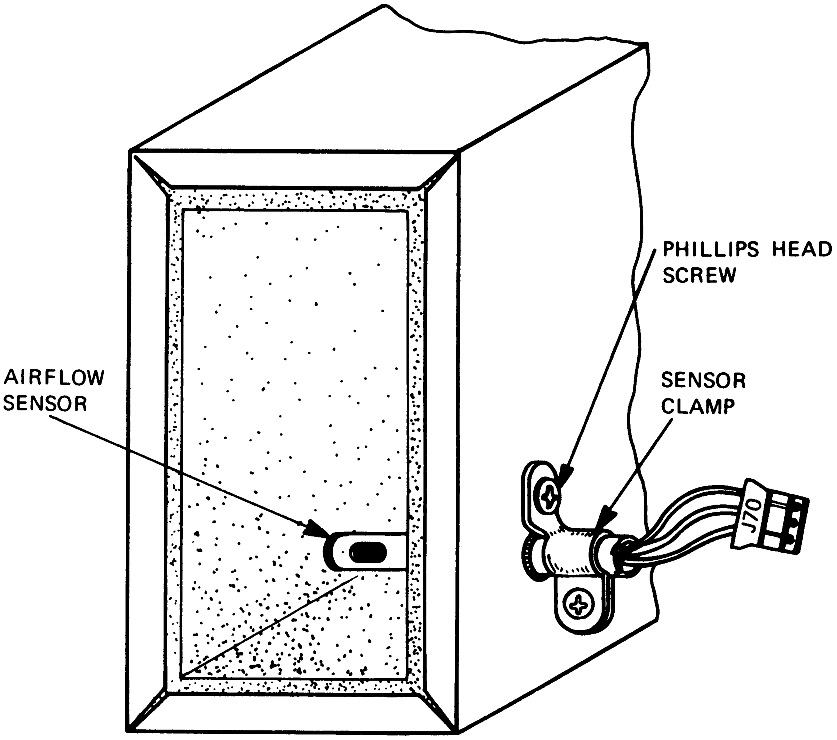


Figure 3-7 Airflow Sensor Assembly Removal

3.13 POWER CONTROLLER

The power controller must be removed to replace either of the power supplies.

1. Open the back door.
2. Remove ac power by placing CB1 in the off position (Figure 3-8).
3. Unplug the power controller from the power source.
4. Remove the two top screws and then the two bottom screws securing the power controller to the cabinet (Figure 3-8). While removing the two bottom screws, push up on the power controller to take the weight off the screws.

CAUTION

Do not pull the power controller out too far because cables are connected to the back.

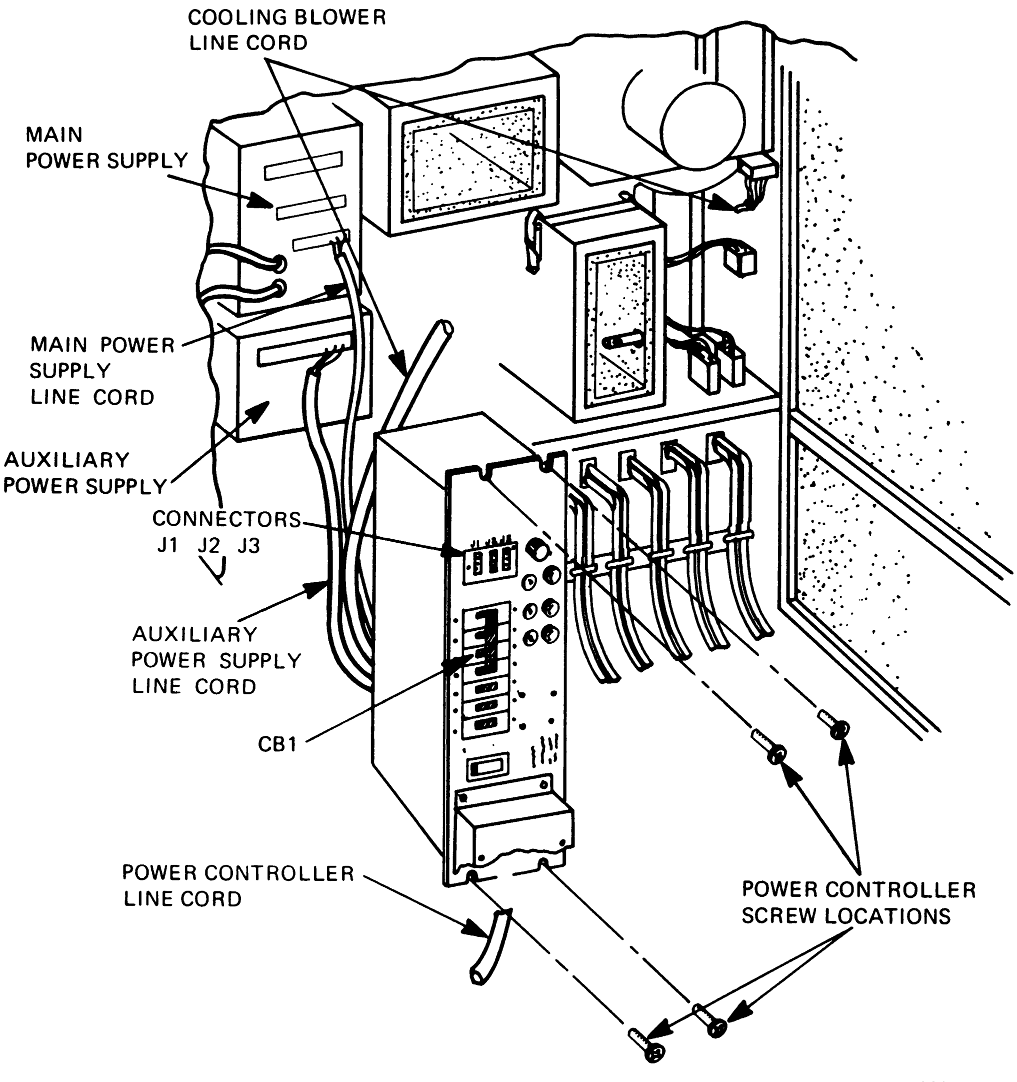

COOLING BLOWER LINE CORD
MAIN POWER SUPPLY
MAIN POWER SUPPLY LINE CORD
AUXILIARY POWER SUPPLY
CONNECTORS J1 J2 J3
AUXILIARY POWER SUPPLY LINE CORD
CB1
POWER CONTROLLER LINE CORD
POWER CONTROLLER SCREW LOCATIONS
CX–024B

Figure 3-8 Power Controller Removal

5. Remove rear door latch to allow clearance for power controller removal.
6. Pull the power controller towards you and then out.
7. For the 60 Hz unit, remove the power control bus cables from J1, J2, and J3 connectors at the front of the power controller. Refer to Figure 2-7. For the 50 Hz unit, refer to Figure 2-8, connectors J1 and J2.
8. Disconnect the ground lead from the screw at the rear of the power controller.
9. Disconnect all line cords from the back of the power controller.
10. Reverse the removal procedure to replace the power controller.

3.14 MAIN POWER SUPPLY

1. Open the back door using a 5/32-inch hex wrench.
2. Turn off CB1 (ac power) on the power controller.
3. Unplug the power controller from the power source.
4. Remove the front door.
5. Remove the power controller (paragraph 3.13) to access the back of the power supply.
6. Unplug the main power supply line cord at the power controller.
7. Disconnect the cable from the −V1 stud (ground) on the back of the power supply (Figure 3-9).
8. Disconnect the cable from the +V1 stud (+5 volts) on the back of the power supply.
9. Disconnect the four orange wires (−5.2 volts) from the −V2 stud on the back of the power supply.
10. Disconnect the four black wires (ground) from the +V2 stud.
11. Unplug J31 (+12 Vdc output from the supply to backplane).
12. Unplug P32 (+12 Vdc and +5 Vdc sense lines). Ensure the P32 cable is free to be removed with the power supply.
13. Unplug J33 (to DC Power switch on maintenance access panel).
14. Unplug J34 (remote on/off jumper to auxiliary power supply).
15. Unplug J35 (+12 Vdc power to the airflow sensor).
16. Turn the four captive screws on the front of the power supply counterclockwise (Figure 3-10).
17. Pull the power supply out about an inch. Check the back of the cabinet to ensure the cables are clear.

CAUTION

This power supply is heavy. Support it with both hands to prevent dropping it.

18. Carefully pull the power supply all the way out of the cabinet.
19. Reverse the removal procedure to replace the main power supply.

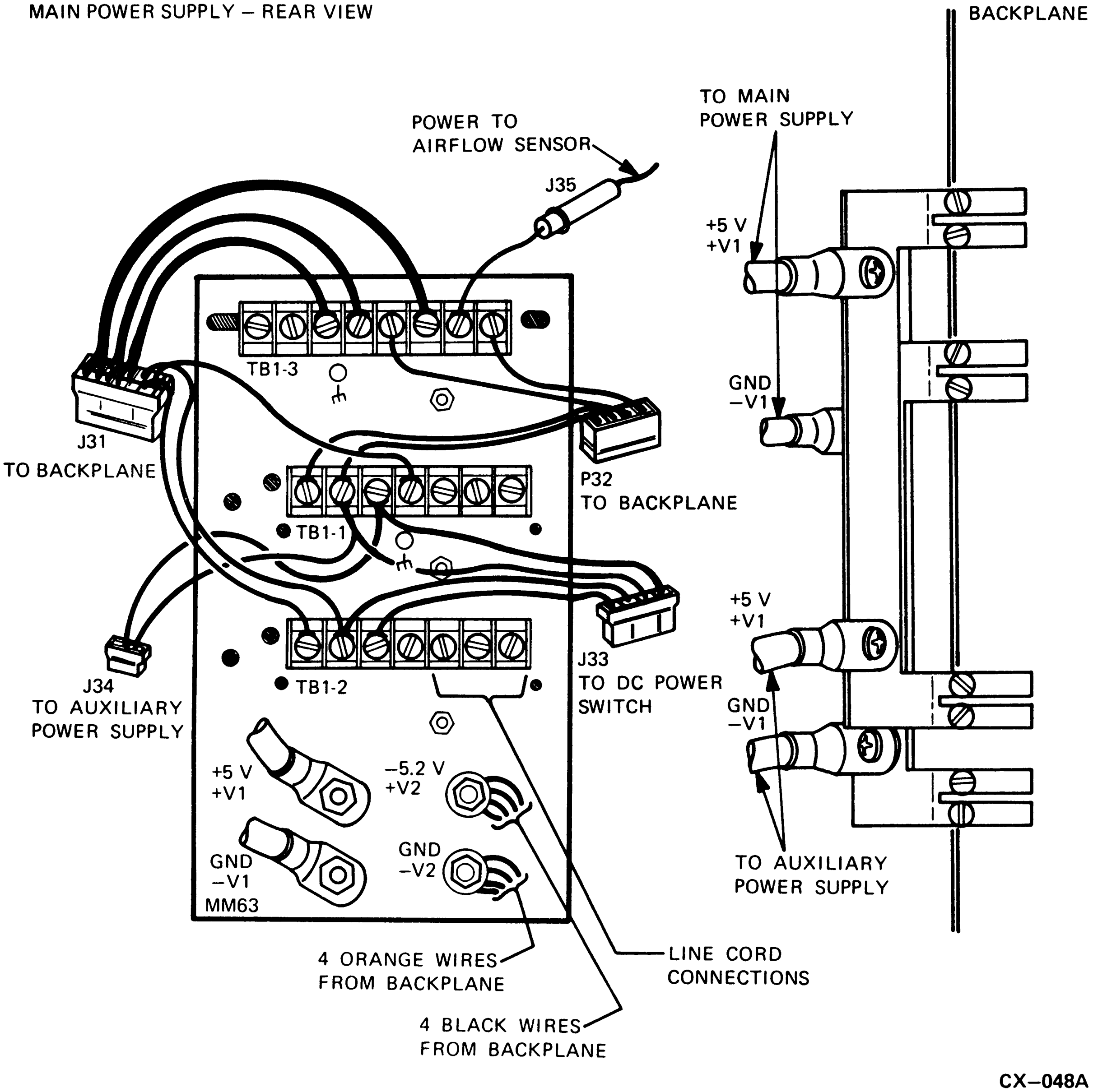


Figure 3-9 Main Power Supply Cables – Disconnection

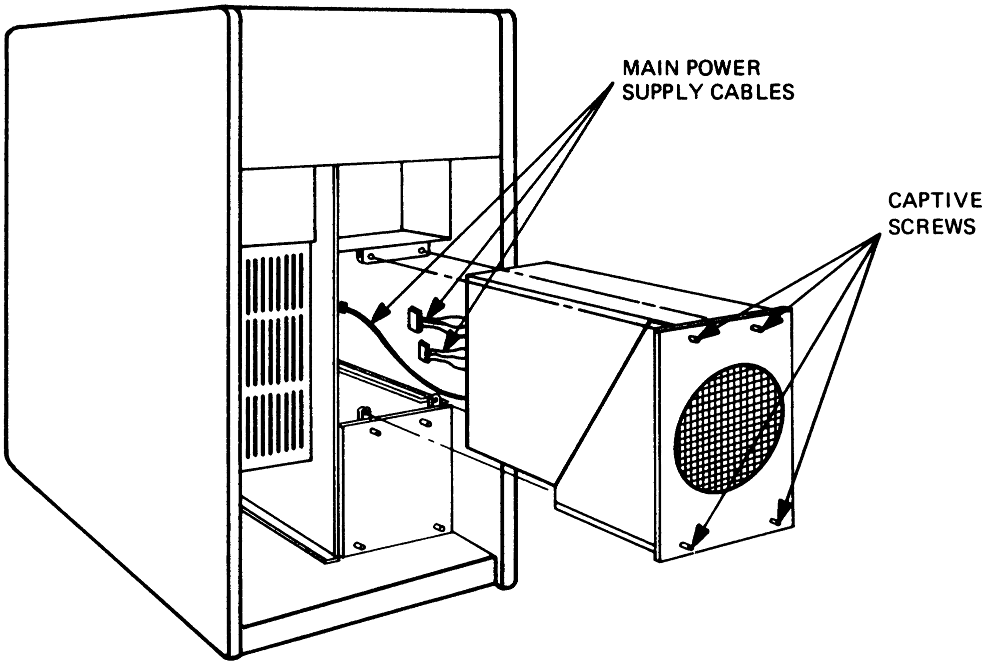


Figure 3-10 Main Power Supply Removal

3.15 AUXILIARY POWER SUPPLY

An HSC50 requires an auxiliary power supply if the total module count in the card cage is more than eight. The auxiliary power supply is mounted directly beneath the main power supply.

1. Open the back door using a 5/32-inch hex wrench.
2. Turn off CB1 (ac power) on the power controller.
3. Unplug the power controller from the power source.
4. Remove the front door.
5. Remove the power controller to access the back of the power supply.
6. Unplug the auxiliary power supply line cord at the power controller.
7. Disconnect the cable from the +V1 stud (+5 volt) on the back of the power supply (Figure 3-11).
8. Disconnect the cable from the −V1 stud (ground) on the back of the power supply.
9. Disconnect J50 (sense line to voltage comparator).
10. Disconnect J51 (dc on/off jumper).
11. Turn the four captive screws on the power supply counterclockwise (Figure 3-12).
12. Carefully slide the power supply out through the front of the HSC50.
13. Reverse the removal procedure to replace the auxiliary power supply.

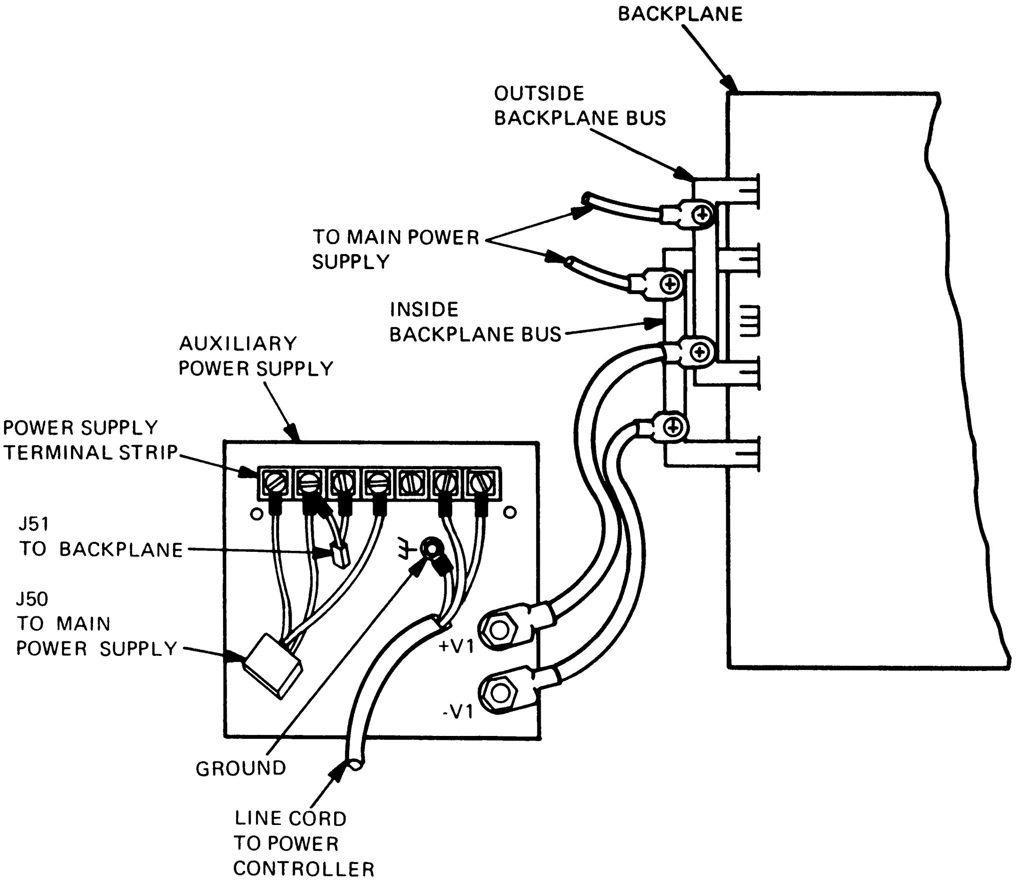


Figure 3-11 Disconnecting Auxiliary Power Supply Cables

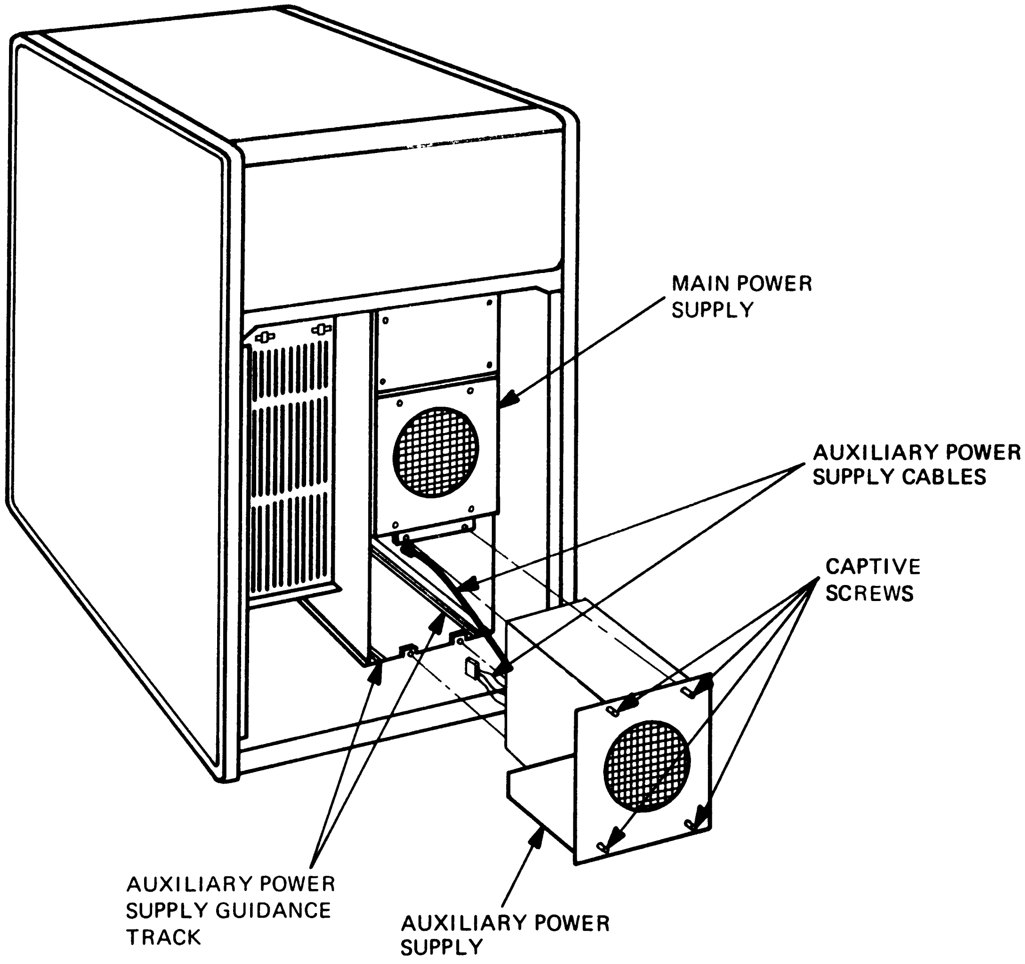

MAIN POWER SUPPLY
AUXILIARY POWER SUPPLY CABLES
CAPTIVE SCREWS
AUXILIARY POWER SUPPLY GUIDANCE TRACK
AUXILIARY POWER SUPPLY
CX–028B

Figure 3-12 Auxiliary Power Supply Removal

BLANK

CHAPTER 4
DIAGNOSTICS AND UTILITIES

4.1 INTRODUCTION

Tests of varying complexity are included in the HSC50 diagnostics and utilities. Running these tests requires an auxiliary or maintenance terminal. This chapter describes installation of the auxiliary terminal, the four types of diagnostic testing and the HSC50 utilities.

For further diagnostics and utilities information, refer to the following:

- *HSC50 Inline Diagnostics User Documentation*
- *HSC50 Offline Diagnostics User Documentation*
- *HSC50 Utilities User Documentation*

4.2 AUXILIARY TERMINAL CONNECTION

Detailed information on LA12 terminal installation and operation is found in the *DECwriter Correspondent Technical Manual.*

Figure 4-1 shows the placement of the two ASCII ports on the HSC50. The auxiliary terminal can connect to either the rear or the front ASCII port.

Two terminals cannot simultaneously connect to an HSC50. The auxiliary terminal should not be installed with HSC50 power on. If power must be left on while connecting the terminal, use the following procedure:

- Put the Secure/Enable switch in the SECURE position.
- Change terminal state (e.g. plug in, remove power, connect EIA line, etc.)
- Type three space characters on the terminal keyboard.
- If it is necessary to put the Secure/Enable switch in the ENABLE position, do so at this point.

If this procedure is not followed, the HSC50 may enter micro-Online Debugger Tool (ODT) mode. This mode is indicated by an @ symbol on the screen. Typing a **P** (proceed) should exit this mode.

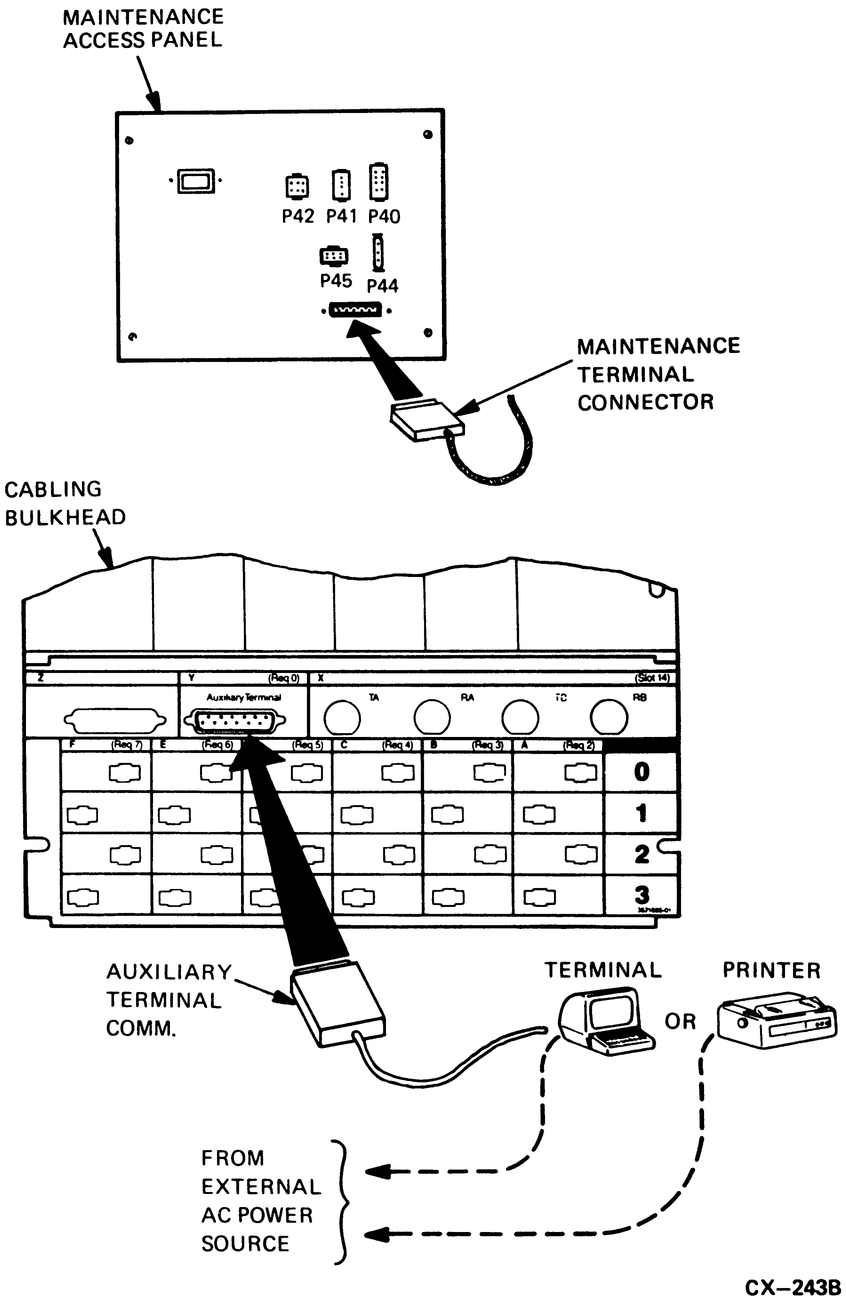


Figure 4-1 Connecting an Auxiliary Terminal

4.2.1 LA12 Parameters

When an LA12 is used as an auxiliary terminal, the following parameters must be established:

1. Communications
    - Auto – Ansbk = no
    - Buffer = 1024
    - Comm Port = EIA
    - Disk – HDX = none
    - Echo – Local = no
    - Fault = none
    - G – HDX Start Mode = Rcv
    - H – Hi Speed (bps) = 9600
    - L – Lo Speed (bps) = 300
    - M – Line Prot = FDX – Data Leads
    - O – Rcv Error Ovride = no
    - Parity = 7/M
    - Q – SRTS Polarity = lo
    - Restraint = Xon/Xoff
    - S – Speed Select = hi
    - Turn Char = none
    - U – Power Up = line
    - V – Frequency = bell 103
2. Keyboard
    - Auto – Linefeed = no
    - Break = yes
    - C – Keyclick = no
    - Keypad = normal
    - Language = USA
    - Repeat = yes
3. Printer
    - A – G0 Char Set = USA
    - B – G1 Char Set = USA
    - C – G2 Char Set = USA
    - D – G3 Char Set = USA

- End-of-line = wrap
- Form Length = 264
- G – Print Cntrl Chars
- Horiz Pitch (CPI) = 10
- Newline Char = none
- Print Force = hi
- Vertical Pitch (LPI) = 6

4.3 BOOTING PROCEDURES

The following paragraphs describe the booting procedures for the System and Offline Diagnostics tapes.

4.3.1 Booting the System Tape

In order to run the HSC50 inline diagnostics and utilities, the HSC50 operating software must be booted with both the System and Utilities cassettes loaded in the TU58 drives. Before inserting the System tape into the TU58 drive, check the black RECORD tab. This tab must be in the record position (as indicated by an arrow on the tab) to ensure proper system operation. The Utilities tape need not be write enabled.

NOTE

Customarily, the System tape resides in TU58 drive 0; however, drive 1 and drive 0 are identical and tape placement is arbitrary.

A boot of the System tape can be initiated by either powering on the unit if it is powered down or, if power is already applied, by depressing and releasing the Init switch with the Secure/Enable switch in the ENABLE position. This causes the P.ioc bootstrap ROM tests to run and then load the Init P.ioc test.

4.3.2 Booting the Offline Diagnostics Tape

The Offline diagnostics tape can be booted in either TU58 drive and need not be write enabled. The Offline tape can be booted by either powering on the unit or depressing and releasing the init switch with the Secure/Enable switch in the ENABLE position. This causes the P.ioc bootstrap ROM tests to run and then load the Offline P.ioc Test.

4.4 HSC50 DIAGNOSTICS

All HSC50 diagnostics execute within the subsystem. No HSC50-specific diagnostics are executed by the host CPU.

Subsystem diagnostics are categorized as follows:

- Powerup bootstrap diagnostics
- Inline diagnostics
- Offline diagnostics
- Periodic diagnostics

These diagnostics reside on the three TU58 tapes shipped with the HSC50. The Inline Diagnostics are contained on the System and Utilities tapes. The Offline diagnostics are found on the Offline Diagnostics tape.

4.4.1 Powerup Bootstrap Diagnostics

These diagnostics include the P.ioc ROM Bootstrap diagnostic and the Init P.ioc diagnostic, described in the following paragraphs.

4.4.1.1 P.ioc ROM Bootstrap Diagnostic – The P.ioc bootstrap diagnostics are executed each time the subsystem is powered up or the Init switch is activated with the Secure/Enable switch in the ENABLE position. These ROM-based diagnostics test the F-11 CPU, part of the P.ioc Program memory and the TU58. Following these tests, the next part of the bootstrap sequence is loaded from the TU58. If the System tape is being booted, the Init P.ioc diagnostic is loaded. If the offline tape is being booted, the Offline P.ioc diagnostic is loaded.

The P.ioc ROM bootstrap diagnostics perform the following:

- Test the basic F11 instruction set and addressing modes.
- Test the Bank and Board Swap bits.
- Test the first 2048 bytes of program memory (vector area).
- Find a working 8K-word partition in program memory.
- Load the Init P.ioc test into the 8K-word partition of program memory if the System tape is being booted.
- Load the Offline P.ioc test into the 8K-word partition of program memory, if the Offline tape is being booted.

Two types of ROM Bootstrap diagnostic failures can occur:

- A failure in the early ROM bootstrap tests causes the F11 to hang, executing a BR . instruction. If the Init lamp fails to light, this type of failure is indicated.
- A failure in later ROM bootstrap tests, after the Init lamp turns on, generates a fault code. The Fault indicator lights upon detecting this type of failure.

For a detailed description of the boot process, refer to the HSC50 Boot Flowchart in Chapter 5.

4.4.1.2 Init P.ioc Diagnostic – The Init P.ioc Test is loaded by the the P.ioc ROM bootstrap test each time the HSC50 System tape is booted. This diagnostic completes the testing of the P.ioc module and the HSC50 memories. At the successful completion of these tests, the HSC50 operating software is loaded and started.

Logic in the following areas is tested with the Init P.ioc diagnostic:

- I/O Control Processor – The rest of the instruction set not tested by the ROM bootstrap, interrupts, memory management, and the control memory lock-cycle circuitry are included. Detected failures result in an error code display on the OCP. (Refer to the fault code chart in Chapter 5.)
- Memory – Program memory is tested from the I/O control processor. However, the control and data memories are tested by the highest-numbered available requestor controlled by the I/O control processor. Again, detected failures result in an OCP error code display.

- Host Interface and Data Channels – Module status is collected and placed in a table for the HSC50 operating software initialization process. As each module is enabled, it automatically executes internal microdiagnostics. These internal diagnostics test the following:
    - ROM (sequencer, checksum, parity, etc.)
    - Special logic unique to that particular module

Upon completion of diagnostics for each module, a status code is passed to the I/O control processor. Status codes for the various modules are discussed in Chapter 5.

If the module diagnostics complete successfully, the status code represents the module type and the module green LED is on. If the diagnostics fail, the status code indicates the failing microtest. In addition, detected failures cause a red LED to light on that module. K.ci and K.sdi/K.sti failures are also displayed on the auxiliary terminal after the boot is completed.

For a detailed description of the boot process refer to the HSC50 Boot Flowchart in Chapter 5.

The user's document for the Init P.ioc Test is contained in the *HSC50 Inline Diagnostics User Documentation* manual.

4.4.1.3 Offline P.ioc Test – The offline P.ioc test is loaded each time the offline diagnostics tape is booted and tests all I/O control processor logic not tested by the bootstrap program. The test runs in a stand-alone environment and provides specific error messages for the isolation of I/O control processor module failures. If the entire test runs with no errors, the offline diagnostic loader is read to memory from the TU58 and started.

For a detailed description of the boot process refer to the HSC50 Boot Flowchart in Chapter 5.

A complete user document on the Offline P.ioc Test is contained in the *HSC50 Offline Diagnostics User Documentation* manual.

4.4.2 Inline Diagnostics

Inline diagnostics, discussed in following paragraphs, include ILDISK, ILTAPE, ILTCOM, ILEXER, ILTU58, and ILMEMY. Although not a diagnostic, CI Responder is included at the end of this section. The inline diagnostics are run when the HSC50 operating software is loaded and run concurrently with other operating system processes. For version V200 of the HSC50 operating software, all inline diagnostics reside on the Utilities tape with ILTU58 also residing on the System tape.

NOTE

Placement of the inline diagnostics on earlier versions of the HSC50 software tapes, V100 and V110, are not the same as for V200. Use the DARE DDn: command (where n equals the TU58 drive number to determine on which tape a particular inline diagnostic resides.)

Inline diagnostics are initiated by typing the command:

```
RUN DDN:TEST NAME
```

where n indicates either drive 0 or drive 1.

Complete user documentation for the inline diagnostics is contained in the *HSC50 Inline Diagnostics User Documentation* manual.

4.4.2.1 ILDISK Diagnostic – ILDISK, known as IDDD on HSC50 software version V100, tests any disk drive connected to an HSC50 not online to any host. ILDISK runs concurrently with other HSC50 software processes using disk functional code subroutines for testing disk drives. The SDI interface and the drive Read/Write electronics are tested, in addition to drive diagnostics execution.

ILDISK can be used to diagnose and isolate drive failures to a field replaceable unit (FRU). This FRU can be the disk data channel module connected to the drive, the SDI cable, or the drive itself.

4.4.2.2 ILTAPE Diagnostic – ILTAPE tests a specific tape formatter dedicated to the test. This diagnostic initiates all formatter-resident diagnostics and executes a series of I/O operations (positioning, reads, and writes) on the transports connected to that formatter. ILTAPE provides 80 percent fault isolation between the formatter, the STI interconnect, and the transport. The error detection capabilities for the drive under test are strictly limited by the self-test diagnostics contained within the transport.

4.4.2.3 ILTCOM Diagnostic – ILTCOM is an inline compatibility test for tapes possibly written on different systems and different drives. This diagnostic tests such tapes for compatibility with STI TA78 drives connected to an HSC50. ILTCOM may generate, modify, read or list a compatibility tape. Compatibility tapes contain files (called bunches) of records with specific data patterns. Data read from the compatibility tape is compared to the expected pattern.

Each bunch on a compatibility tape contains a header record and several data records differing in size. Each bunch is terminated by a Tape Mark. The last bunch on a tape is followed by an additional Tape Mark (logical EOT). In addition, each bunch contains a total of 199 records: one header record followed by 198 data records.

4.4.2.4 ILEXER Diagnostic – ILEXER, known as OMDEXR in version V100, simultaneously exercises up to 12 disk and/or tape drives. The exercise contains random drive sequences, data patterns and operation sequences. Operations and errors are counted for statistical reporting. Subsystem error handling, error reporting, and correction features are employed. ILEXER does not provide for fault isolation or for initiation of bad block replacement.

4.4.2.5 ILTU58 Diagnostic – ILTU58 tests any TU58 drive attached to the HSC50. An operator can initiate this test using the auxiliary terminal with only the System tape installed. ILTU58 is also resident on the Utilities tape.

Because the HSC50 operating software tests the TU58 each time it is used, ILTU58 performs only minimal testing. Several Read and Write operations are performed to test the internal data paths and Read/Write electronics of the TU58. It is not necessary to use a scratch tape when running this test.

Only the TU58 and the serial data path between it and the I/O control processor are tested by this diagnostic. All other system hardware is assumed to be operational.

4.4.2.6 ILMEMY Diagnostic – The inline memory diagnostic, ILMEMY, tests HSC50 data memory data buffers that failed during system operation. This test can be initiated automatically or upon demand. The test is initiated automatically by the HSC50 operating software to test data buffers that produced a parity error or NXM when in use by the HSC50 operating software. Buffers that fail the memory test are removed from service by sending them to a disabled buffer queue. Buffers sent twice to this test are sent to the disabled buffer queue even though they did not fail. Buffers that pass the memory test are sent to a free buffer queue for further use by the HSC50 operating software.

When this test is initiated on demand, any buffers on the disabled buffer queue are tested, and the results of the test are displayed on the terminal from which the test was initiated.

4.4.2.7 CI Responder – CI Responder (RS) simulates traffic on the CI bus. It is not a diagnostic but a tool for monitoring and performing CI transactions. This program responds only to commands from the CI Exerciser (CIE), based in a host CPU.

HSC50s running V110 (or higher) firmware are shipped with the responder ready to load and execute automatically. The SETSHO command, SHO LOAD, indicates if the CI Responder is loaded. Additional information on CI Responder is found in the VAX/VMS documentation defining cluster tests.

4.4.3 Offline Diagnostics

Offline diagnostics, not previously discussed as part of the bootstrap process, are described in the following paragraphs. Included are the Offline Diagnostic Loader, TEST MEM, TEST MEM BY K, TEST K, TEST BUS, TEST OCP, and TEST REFRESH. Offline diagnostics are found on the Offline Diagnostics tape and in the *HSC50 Offline Diagnostics User Documentation*.

4.4.3.1 Offline Diagnostic Loader – The offline diagnostic loader is loaded by the offline P.ioc test when it detects no errors. It is used to load the offline diagnostics. The following is displayed on the HSC50 console to indicate the offline loader has been successfully loaded.

```
HSC50 OFL DIAGNOSTIC LOADER
RADIX=OCTAL, DATA LENGTH=WORD, RELOC=00000000
ODL>
```

The message indicates the offline loader is ready to accept any of the following commands:

- **HELP** – This command provides an abbreviated list of all commands recognized by the loader. In response to the HELP command, the loader reads the file **OFLLDR.HLP** from the TU58 and displays the file contents on the auxiliary terminal.
- **LOAD** – This command loads, but does not start, a program into HSC50 program memory. Command format is LOAD <filename> where <filename> is the name of any file on the HSC50 Offline Diagnostics tape. The loader program finds the specified file and loads it into program memory.
- **START** – This command directs the loader to initiate the program currently loaded in program memory. The START command can be used in conjunction with the preceding LOAD command or it can reinitiate the last offline diagnostic. Using the START command is much faster than reloading the program from the TU58.
- **EXAMINE** – This command displays the contents of any location in HSC50 program, data, or control memories. Command format is **EXAMINE <address>** where **<address>** can be a string of digits in the current (default) radix. Certain symbolic addresses are also permitted. For example:

  ```
  ODL > )E 14017776 <CR >
  (D) 14017776 125252
  ```

  In this example, the command EXAMINE (abbreviated to E) requests the contents of location 14017776. When the loader displays this information, the address is preceded by a (D) indicating the location is within HSC50 data memory. Finally, the example states the location contains the value 125252.
- **DEPOSIT**– This command modifies the contents of any location in HSC50 program, control, or data memories. The format of the command is:

  ```
  DEPOSIT <ADDRESS> <DATA>
  ```

where **<address>** can be a string of digits in the current (default) radix. Certain symbolic addresses are also permitted. An example is:

```
ODL> D 14017776 123456<CR>
```

In this example, the command stores the value 123456 into the contents of address 14017776. The previous contents of this data memory location are replaced with the value specified in the DEPOSIT command (123456).

- **SIZE** – This command invokes the Offline System Sizer program. The program determines the sizes of the three HSC50 memories, the status of each requester, and the type of module in each HSC50 requestor number. This requestor number refers to module priority on the data and control memory buses. It does not necessarily correspond to module slot numbers.
- **TEST** – This command invokes the various available offline diagnostics. For more information, refer to the *HSC50 Offline Diagnostics User Documentation* manual.

4.4.3.2 TEST MEM – By operator selection, TEST MEM exercises either the control, data, or program memory. Three memory testing algorithms are used: the quick verify algorithm, the moving inversions algorithm, and the walking ones algorithm. These algorithms stress the memories to detect transient errors caused by bus and memory timing problems. Errors are reported on the auxiliary terminal as they occur. After reporting a data error or a parity error in the location under test, the diagnostic continues. The program restarts from the beginning if a nonexistent memory (NXM) error occurs while initially clearing memory. However, testing continues if a NXM occurs during the memory test.

4.4.3.3 TEST MEM BY K – TEST MEM BY K uses one of the data channel requestors or the port processor requestor to test data or control memory. This diagnostic runs faster than the offline memory diagnostic. Because requestors lack an interface to the program memory bus, this diagnostic cannot test program memory.

The test algorithm stresses the memories attempting detection of transient errors caused by bus and memory timing problems. Errors are displayed on the terminal screen as they occur.

4.4.3.4 TEST K – TEST K executes from the I/O control processor. This test uses the HSC50 K control area to direct self-testing of a K module. The operator selects the module and the microdiagnostic test to be executed (Tables 4-1, 4-2, and 4-3). Errors are reported on the auxiliary terminal as they occur. Successful completion of preceding tests, as well as operability of the P.ioc, program memory and TU58, is assumed.

Table 4-1 K.ci Microdiagnostics

Test Number	Name
000	Sequencer test
001	ALU test
002	Data bus test
003	Control bus test
004	PROM parity test
005	Memory test (not available on demand)
006	RAM test
007	PLI interface test
010	Packet buffer test
011	Link test

Table 4-2 K.sdi Microdiagnostics

Test Number	Name
000	Sequencer test
001	ALU test
002	Data bus test
003	Control bus test
004	PROM parity test
005	Memory test (not available on demand)
006	RAM test
007	SERDES/RSGEN test
010	Partial SDI interface test

Table 4-3 K.sti Microdiagnostics

Test Number	Name
000	Sequencer test
001	ALU test
002	Data bus test
003	Control bus test
004	PROM parity test
005	Memory test (not available on demand)
006	RAM test
007	SERDES test
010	Partial STI interface test

4.4.3.5 TEST BUS – The HSC50 Offline Bus Interaction test (TEST BUS) is an HSC50 system exerciser. The bus interaction test creates control and data bus contention among the HSC50 requestors. Such contention is generated by different requestors simultaneously testing different portions of the same memory. In the memory testing process, the various requestors contend with each other for use of control and data memories.

While the requestors are generating bus contention, the I/O control processor is exercising the OCP, TU58, and all three HSC50 memories.

To operate this test, a minimum of two working requestors is required (one is the P.ioc). It uses a maximum of seven requestors if they are available. As the number of available requestors increases, so does bus contention. The run time of this test increases linearly as the number of requestors is increased. In addition, a larger number of requestors facilitate problem isolation to a particular source. Errors are displayed on the auxiliary terminal as they occur.

4.4.3.6 TEST OCP – TEST OCP checks the operation of the HSC50 indicators and switches including the five OCP switches and indicators, the State LED, the Secure/Enable switch, the Power LED, and the Enable LED.

4.4.3.7 TEST REFRESH – TEST REFRESH finds memory problems related to refresh capabilities. Patterns are written to memory and then checked after a one-minute interval. Three separate patterns test each memory bit (including parity bits) in the ones state and in the zero state. REFRESH completes each pass within three minutes.

All three HSC50 memories are tested although only the program and control memories require refreshing. Tests of data memory are included because some static RAM failures resemble refresh problems.

The refresh test can find problems in the memories undetected by routine memory tests. This test is not intended for memories failing standard memory tests.

4.4.4 Periodically-Scheduled Diagnostics

Periodically-scheduled diagnostics are run automatically when the subsystem is performing little or no I/O. These tests run very quickly (tens of milliseconds) avoiding throughput impact.

Normally, HSC50 periodic diagnostics are enabled by default with a one-minute time interval. This interval is the minimum time required between successive calls to run any periodic diagnostic. To confirm periodic diagnostics are enabled, use the utility command **SHO SYSTEM.**

The **SET PERIODIC__DIAGNOSTICS [time-interval]** command enables the periodic diagnostics. The periodic diagnostics are:

- **PRKSDI** – K.sdi Diagnostic
- **PRKSTI** – Currently not implemented
- **PRMEMY** – Memory Diagnostic

PRKSDI and **PRKSTI** run a particular microdiagnostic on each of the available K.sdi and K.sti modules. A different diagnostic runs with successive calls to this routine. If this series of tests executes successfully, the process is transparent to the user.

PRMEMY tests the following:

- Control bus transceivers
- Data bus transceivers
- Memory parity-checking circuits

Periodic diagnostic failures and error messages are found in Chapter 5.

4.5 HSC50 UTILITIES

HSC50 utilities are stored on the TU58 Utility tape and include:

- SET/SHOW
- TUCOPY
- TPATCH
- FORMAT
- VERIFY
- BACKUP
- RESTORE

A utility program executes after typing the word RUN followed by the program name. A ^ Y (control Y) must be keyed on the terminal to obtain the command prompt, HSC50 > .

Descriptions of the utility programs follow. For more details, refer to the *HSC50 Utilities User Documentation* and the *HSC50 User Guide*.

4.5.1 SET/SHOW

This program allows the modification or display of any subsystem parameter. Details of each SET/SHOW command are presented in the *HSC50 Users Guide*. The following are the valid SET/SHOW utility commands:

- **SET (desired parameter)** allows parameter to be changed.
- **SHOW (desired parameter)** allows parameter to be displayed.
- **HELP SET** displays all of the valid SET commands.
- **HELP SHOW** displays all of the valid SHOW commands.
- **HELP** displays all of the valid SET or SHOW commands.
- **Control Z (^ Z)** takes default values for as many consecutive optional parameters as possible and prompts for nondefaultable parameters if any.
- **EXIT** exits the SET/SHOW process after updating the system configuration table (SCT) on the TU58 if necessary. If the changes warrant a system reboot, the command issues the following prompt:

  ```
  REBOOTING HSC; Y TO CONTINUE, CONTROL Y TO ABORT:
  ```

- **Control C (^ C)** or **control Y (^ Y)** exits the SETSHO utility without any change in the HSC50 SCT.

4.5.2 TUCOPY

This program allows TU58 tape duplication, a field service responsibility. At least one backup copy of each tape (System, Utilities, and Offline Diagnostics) should be available at all times. A description of TUCOPY user prompts is found in the *HSC50 Utilities User Documentation*.

4.5.3 TPATCH

This utility allows the patching of TU58 tape programs. Each software patch release is shipped with step-by-step directions.

4.5.4 FORMAT

This program reformats the specified disk unit and can destroy all previously written files. Because the disk to be reformatted is dedicated to this program, all disk files must be backed up on another media. As faulty sectors are found, the format program replaces them.

Note that Version V100 software requires a password to format the user data area. Without the password, only the DBN space is formatted. A password is not required with versions V110 or higher.

4.5.5 VERIFY

This program is used to verify disk integrity following disk reformatting. All discrepancies and faulty blocks are reported. Information on revectoring and block replacements is summarized. No user data is destroyed.

4.5.6 BACKUP

The BACKUP utility is used to physically back up disk data onto magnetic tape. For more information, refer to the operating software release notes shipped with each HSC50, the *HSC50 User Guide*, and the *HSC50 Utilities User Documentation*.

4.5.7 RESTORE

Used in conjunction with BACKUP, the RESTORE utility is used to retrieve backed up data from tape for disk storage. For more information, refer to the operating software release notes shipped with each HSC50, the *HSC50 User Guide*, and the *HSC50 Utilities User Documentation*.

CHAPTER 5
PROBLEM ANALYSIS AIDS

5.1 INTRODUCTION

This chapter describes various aids in HSC50 problem analysis including:

- OCP fault code chart and interpretation
- Troubleshooting
- Software crash interpretations
- Status and event codes
- Tape drive related errors
- Power system
- Internal cabling

5.2 OPERATOR CONTROL PANEL FAULT CODE CHART

Figure 5-1 shows the settings for OCP fault code displays. The following paragraphs interpret these codes.

	HEXA-DECIMAL	OCTAL	OCP INDICATORS				
			INIT	FAULT	ONLINE		
PORT PROCESSOR MODULE *	01	01	OFF	OFF	OFF	OFF	ON
DISK DATA CHANNEL *	02	02	OFF	OFF	OFF	ON	OFF
TAPE DATA CHANNEL *	03	03	OFF	OFF	OFF	ON	ON
I/O CONTROL PROCESSOR MODULE FAILURE	11	21	ON	OFF	OFF	OFF	ON
MEMORY MODULE FAILURE	12	22	ON	OFF	OFF	ON	OFF
TU58 FAILURE	13	23	ON	OFF	OFF	ON	ON
PORT LINK MODULE FAILURE (INCORRECT SWITCH SETTING)	15	25	ON	OFF	ON	OFF	ON
MISSING REQUIRED FILES	16	26	ON	OFF	ON	ON	OFF
NO WORKING REQUESTORS IN SUBSYSTEM	18	30	ON	ON	OFF	OFF	OFF
REBOOT BEFORE PREVIOUS BOOT COMPLETE	19	31	ON	ON	OFF	OFF	ON
SOFTWARE DETECTED INCONSISTENCY	1A	32	ON	ON	OFF	ON	OFF

* INCORRECT REVISION OF MICROCODE

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Figure 5-1 Operator Control Panel Fault Codes

5.2.1 Fault Code Chart Error Interpretation

1. OCP codes 1, 2, and 3 (octal) indicate the module contains microcode not compatible with the operating software booted. Check the revision matrix chart in Appendix B for the correct revision levels.
2. OCP error code of 21 (octal) indicates a faulty L0105 module. Replace the L0105 and use the following as a guide:
   - Establish the baud rate. (Refer to section 2.5.3.)
     - Run Bus Interaction Offline diagnostic (TEST BUS) verifying the new module.
3. OCP error code of 22 (octal) indicates the memory tests failed. Use the following as a guide:
   - Possible FRUs are M.std (L0106), P.ioc (L0105) or power supplies.
   - If the memory module is replaced, do the following:
     - Run Offline Memory diagnostic (TEST MEM) for about 30 minutes.
     - Run Bus Interaction Offline diagnostic (TEST BUS).
     - Execute the SHO MEM command.
   - If any memory locations appear in the suspect or disabled memory locations lists, perform the following:
     - Set Secure/Enable switch to ENABLE.
     - Execute SET MEM ENABLE/ALL command.
4. OCP code of 23 (octal) indicates a TU58 problem. If a fault code of 23 occurs during the boot process, more information is available. Use the F-11 online debug tool (ODT) to look at this information. Press BREAK and examine address 172340. It contains the failing test number.

   If Test 4 discovered any TU58 faults, error information is available. Use ODT to examine locations 400 through 412, as follows:

   - 400 = Error code for TU58 controller 0 CSR = 177520 unit 0
   - 402 = Error code for TU58 controller 0 CSR = 177520 unit 1
   - 404 = Error code for TU58 controller 1 CSR = 177530 unit 0
   - 406 = Error code for TU58 controller 1 CSR = 177530 unit 1
   - 410 = Error code for $SLO (normally terminal)
   - 412 = Error code for $SLO (normally not used)

   The low byte contains the error code assigned by the bootstrap. The high byte contains the error code contained in the End packet sent by the TU58 controller, as shown in Table 5-1.

Table 5-1 TU58 Self-Test Error Codes

LOW BYTE

0 = No error
1 = NXM accessing CSR
2 = TU58 sync sequence failed
3 = TU58 failed self-test
4 = Drive did not contain bootable image
5 = Checksum error in received packet
6 = Timeout on Transmitter Ready bit
7 = Timeout on Receiver Done bit
10 = Overrun or framing error
11 = Unknown packet type received

HIGH BYTE

1774xx = Self-test failed
1770xx = End of tape
1750xx = Hard Read error
1740xx = Bad unit number given
1734xx = No cassette mounted
1724xx = Write protected
1674xx = Data check error
1600xx = Seek error
1574xx = Motor stopped
1500xx = Faulty Op Code
1444xx = Faulty block number given

Use the following guide to isolate a TU58 tape/drive/TU58 controller problem:

- Ensure the TU58 controller self-test LED is on. A faulty controller module is indicated if the LED is off.
- Insert backup tape from the same HSC50 into the same drive.
- Reinitialize the HSC50. A faulty tape is indicated if the backup tape passes initialization diagnostics.
- Place the backup tape into the other drive.
- Reinitialize HSC50.
    - A faulty TU58 drive is suspected if the initialization diagnostics run successfully.
    - If these diagnostics fail, an inoperable TU58 controller module is indicated.
    - If these problems are corrected and an error still exists, the fault could be in the +12 V power to the TU58, the P.ioc module, or the harness between the TU58 and the P.ioc.

5. OCP code of 25 (octal) indicates the node address switches on the L0100 module are set to a value greater than F (hex).
6. OCP code of 26 (octal) indicates some of the required files could not be found on the System tape. This could mean a TU58 problem. Refer to the procedures outlined for an OCP code of 23 (octal) in step 4.

7. OCP code of 30 (octal) indicates insufficient working requestors in the HSC50. Use the following as a guide:
   - Replace those L0108 or L0107 modules with a red LED on.
   - Compare the module utilization label on the HSC50 with actual module complement. Check for missing requestors and replace.
   - Restore to its proper place any module in the wrong location.
8. OCP code of 31 (octal) indicates a crash occurred while attempting to load and initialize the HSC50 control program. Use the following as a guide:
   - Depress **BREAK** key on terminal.
   - Key in **177576/**.
   - Analyze bits 8 to 11 of the 16-bit message displayed:
     - **X XXX XXX 1XX XXX XXX** = Nonexistent Memory (NXM) Trap. Probable causes are:
       - I/O control processor module
       - Memory module
       - Software problem
     - **X XXX XX1 0XX XXX XXX** = Illegal instruction. Probable causes are:
       - I/O control processor module
       - Memory module
       - Software problem
     - **X XXX XX1 1XX XXX XXX** = Parity trap. Probable causes are:
       - Memory module
       - I/O control processor module
     - **X XXX X10 0XX XXX XXX** = Level 7 interrupt.
     - **X XXX X10 1XX XXX XXX** = Memory Management Unit (MMU) trap. Probable causes are:
       - I/O control processor module
       - Software problem
     - **X XXX X11 0XX XXX XXX** = Software caused crash.
     - **X XXX 111 XXX XXX XXX** = Host Interface (K.ci) host reset.
     - **X XXX 100 0XX XXX XXX** = User requested a reboot of HSC50.

9. OCP code of 32 (octal) indicates an inconsistency in the software and generally means the System tape must be replaced. This error occurs mainly during the initialization process. Use the following as a guide:
    - Boot, using the backup System tape.
    - If this error occurs while attempting to install a new software revision, return to the previous revision.

5.3 Tape Drive Related Error Messages

Following are examples of tape drive related error messages, defining certain fields as they are printed on the HSC50 auxiliary terminal.

5.3.1 Breakdown of GEDS Text Field

The following is an example of a tape drive related error message printed on the HSC50 auxiliary terminal.

```
ERROR-W TAPE DRIVE REQUESTED ERROR LOG AT 15-AUG-1984 18:43:05.80
      COMMAND REF                  00001D8E
      TA78 UNIT                    20.
      ERR SEQ                      1.
      ERROR FLAGS                  40
      EVENT                        FF6B
      POSITION                     2.
      GEDS TEXT                    7D 02 0014 00000002
      DRIVE ERROR LOG              00 00 00 00 C5 38 04 04
                                   46 FF 07 FF 00 00 00 00
                                   81 00 00 21 FF B0 00 04
                                   00 00 80 FF 17 DE 00 08
                                   00 00 21 FF FF 00 00 99
                                   99 47 F4 E8 00 56 85 19
                                   A2 0A 80 FF 17 DE
```

Both the GEDS Text and Drive Error Log portions of this message result from a GET EXTENDED DRIVE STATUS command to the drive from the HSC50. The Drive Error Log portion can be interpreted by referencing the service manual for the appropriate tape drive. (The preceding example is for a TA78 drive.)

Following is a breakdown of the information contained in the GEDS Text field. The leftmost byte is referenced as the First Byte and the rightmost byte as the Eighth Byte.

Bytes in the GEDS Text field are described as follows:

First Byte = Speed:	Currently sets speed of the drive; it is an integer value in inches per second (IPS) rounded down to the nearest integer. For a totally variable speed drive, the speed returned is the lower bound on the range of permissible speeds. In the example shown, this field contains a value of 7D which corresponds to 125 IPS.
Second Byte = Density:	This is the current operating density of the tape unit. Only one bit is set to indicate the current operating density. 04 = 6250 BPI 02 = 1600 BPI 01 = 800 BPI

Third and Fourth Bytes = Unit Number:	These bytes contain the drive unit number (hex).
Fifth through Eighth Bytes = Gap Count:	This is the number of gaps the formatter believes the tape drive to be from the beginning of tape. The contents of this field may differ from the Position field in this error message. The Position field contains what the HSC50 believes the gap count should be at the end of successful completion of all outstanding commands.

5.3.2 Breakdown of GSS Text Field

Following is another example of a tape drive related error message printed at the HSC50 console.

```
ERROR-E DRIVE DETECTED ERROR AT 18-AUG-1984 12:05:34.82
        COMMAND REF                     0346003
        TA78 UNIT                       3.
        ERR SEQ                         7.
        ERROR FLAGS                     40
        EVENT                           00EB
        POSITION                        0.
        GSS TEXT                        02 20 00 00
                                        28 00 00 00 00 00 14 00

ERROR-I END OF ERROR.
```

The GSS Text field of this error message is the response received by the HSC50 from the tape formatter when the HSC50 issues the GET SUMMARY STATUS (GSS) and TOPOLOGY commands. It is also the unsuccessful response for all Level 2 commands. Following is a breakdown of this response and an interpretation of bits contained in it.

AF	A3	A2	A1	A0	OA	PS	DR	SUMMARY MODE BYTE 1
FE	TE	PE	DF					SUMMARY ERROR BYTE
			PB	EL	RP	RT	FD	SUMMARY MODE BYTE 2
C1	C2	C3	C4	C5	C6	C7	C8	CONTROLLER BYTE
TM	EOT	BOT	WL	OL	AV	MR	EL	DRIVE 0 MODE BYTE
DE	LP	PL	EX	DTE	SME	DI	ZT	DRIVE 0 ERROR BYTE
TM	EOT	BOT	WL	OL	AV	MR	EL	DRIVE 1 MODE BYTE
DE	LP	PL	EX	DTE	SME	DI	ZT	DRIVE 1 ERROR BYTE
TM	EOT	BOT	WL	OL	AV	MR	EL	DRIVE 2 MODE BYTE

DE	LP	PL	EX	DTE	SME	DI	ZT	DRIVE 2 ERROR BYTE
TM	EOT	BOT	WL	OL	AV	MR	EL	DRIVE 3 MODE BYTE
DE	LP	PL	EX	DTE	SME	DI	ZT	DRIVE 3 ERROR BYTE

AF : Formatter Attention Asserted

A3 : Drive 3 Attention Asserted

A2 : Drive 2 Attention Asserted

A1 : Drive 1 Attention Asserted

A0 : Drive 0 Attention Asserted

AV : Drive Available to Formatter

BOT: Beginning of Tape

C*n* : Controller Flags (C1 – C8) – Currently not implemented

DE : Drive Error – asserted when any drive error is detected not covered by other status bits.

DF : Formatter Diagnostic Failed

DI : Diagnostic Mode – when set, instructs the formatter to use special internal algorithms to report imperfect performance.

DR : Diagnostic Requested – asserted when formatter is requesting a diagnostic to be executed by the controller.

DTE: Data Transfer Error – asserted when any error occurs which prevents a data transfer from completing successfully.

EL : Error Logging Request – asserted by either the drive or formatter when error logging information is available.

EOT: End of Tape – asserted when the tape is positioned at or past the end of tape marker.

EX : Exception Condition – asserted whenever the formatter encounters TM, BOT, or EOT during a data transfer operation or when EL is raised during a data transfer.

FD : Retry Bit – Failure / Direction – asserted during error recovery to indicate the direction in which a retry should be made or to indicate a failing operation. If RP = 0 and RT = 1, then FD = direction to transfer. FD = 0 means transfer in the same direction as original operation; FD = 1 means transfer in the opposite direction of original operation. If RP = 1 and RT = 0, then FD indicates success or failure of operation. FD = 0 means the retry sequence succeeded; FD = 1 means the retry sequence failed.

FE : Formatter Error – asserted on formatter errors not covered by the TE, PE, or DF bits. These errors include fatal errors that may turn on the drive fault indicator.

LP : Lengthy Operation in Progress – asserted when a rewind operation including the optional data security erase portion of a rewind) is in progress.

MR : Maintenance Mode Request – asserted when the drive is put into maintenance mode. On the TA78, this is accomplished via a thumbwheel switch on the operator panel.

OA : Formatter Online or Available (for the TOPOLOGY command).

OL : Drive Online to Formatter.

PB : Active Port Button – PB = 0 if formatter is connected to the controller through port A; PB = 1 if formatter is connected to the controller through port B.

PE : Level 2 Protocol Error – asserted when a protocol error is detected while processing a Level 2 command.

PL : Position Lost – asserted when the formatter is not certain of the current tape position.

PS : Port Switch – asserted when the port switch is enabled.

RP : Request Position – used by the formatter along with RT to inform the controller of the next step in the error recovery sequence.

- Retryable RP = 1, RT = 1
- Transfer RP = 0, RT = 1
- Done RP = 1, RT = 0
- No Error RP = 0, RT = 0

RT : Request Transfer – refer to the explanation for RP.

SME: Speed Management Enabled – asserted whenever the formatter may change the current operating speed of a particular drive at any time (provided the changing of the drive operating speed is transparent to the controller).

TE : Transmission Error – used by the formatter to report Level 0 and Level 1 STI errors. The formatter only reports Level 0 real-time state parity errors and Write/Cmd Data Line pulse errors when a transfer is in progress. Level 1 errors are framing errors, checksum errors, inappropriate value in data field of real-time command, or a real-time command occurring in an invalid context.

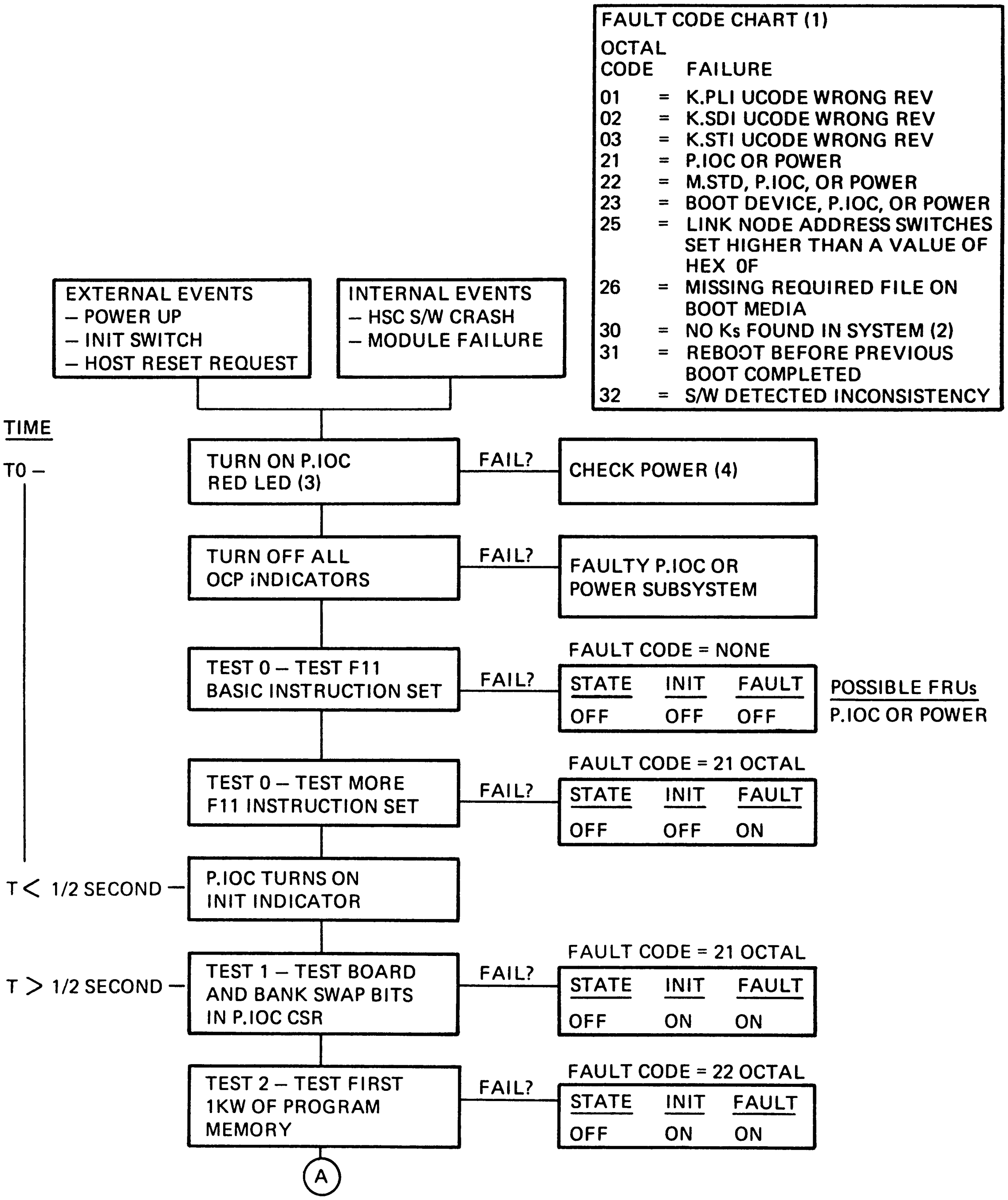
TM : Tape Mark

WL : Write Locked

ZT : Zero Threshold – instructs the formatter to change all error thresholds from their default values to zero.

5.4 TROUBLESHOOTING FLOWCHARTS

Figure 5-2 illustrates troubleshooting for the HSC50 boot process. Figure 5-3 is a troubleshooting flowchart for the power supply.



FAULT CODE CHART (1)

OCTAL CODE		FAILURE
01	=	K.PLI UCODE WRONG REV
02	=	K.SDI UCODE WRONG REV
03	=	K.STI UCODE WRONG REV
21	=	P.IOC OR POWER
22	=	M.STD, P.IOC, OR POWER
23	=	BOOT DEVICE, P.IOC, OR POWER
25	=	LINK NODE ADDRESS SWITCHES SET HIGHER THAN A VALUE OF HEX 0F
26	=	MISSING REQUIRED FILE ON BOOT MEDIA
30	=	NO Ks FOUND IN SYSTEM (2)
31	=	REBOOT BEFORE PREVIOUS BOOT COMPLETED
32	=	S/W DETECTED INCONSISTENCY

NOTE 1: FOR A MORE DETAILED EXPLANATION OF THESE FAULT CODES, REFER TO SECTION 5.2.1 IN THIS MANUAL.

NOTE 2: Ks (REQUESTORS) = K.SDI, K.STI, K.PLI.

NOTE 3: ALL MODULE RED INDICATORS ON EXCEPT MEMORY (NO RED LED ON IT).

NOTE 4: REFER TO POWER SUPPLY TROUBLESHOOTING FLOWCHART (CHAPTER 5).

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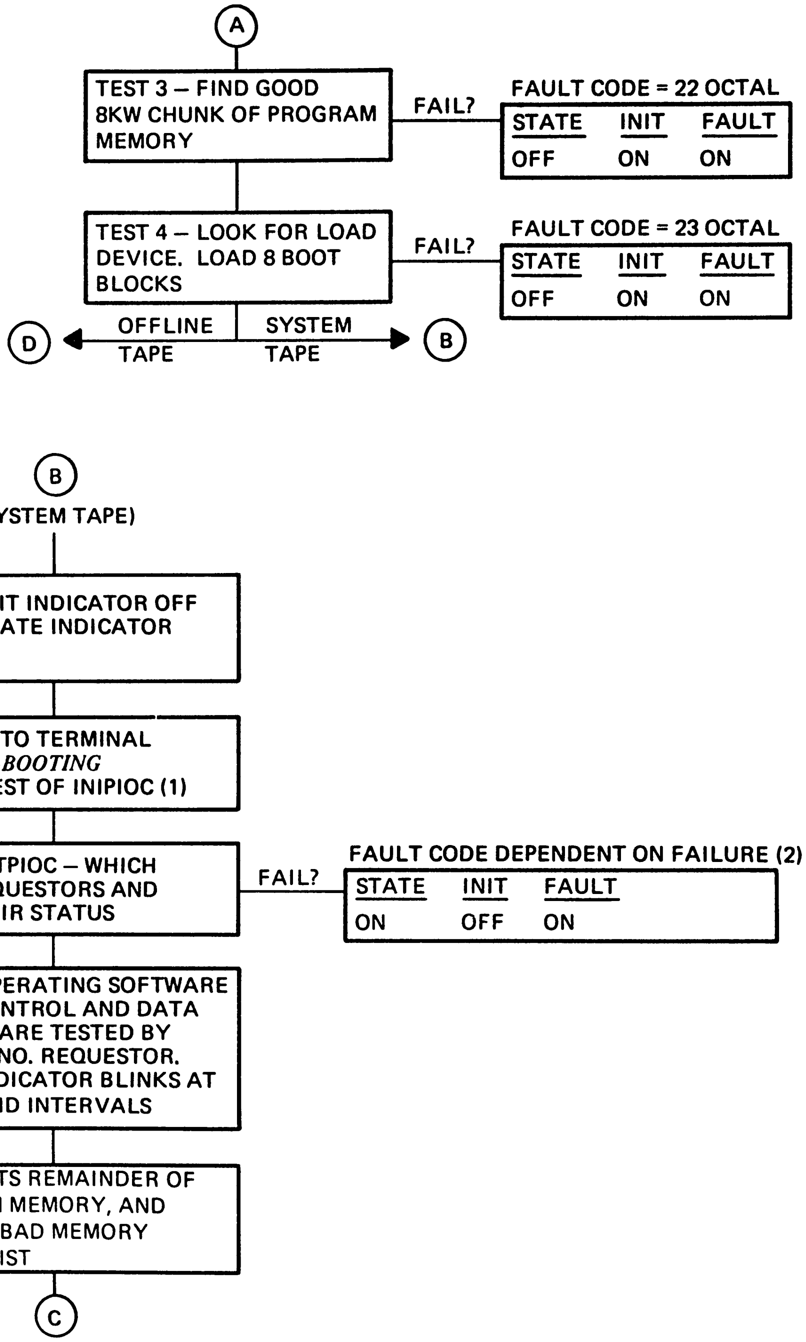
Figure 5-2 HSC50 Boot Flowchart (1 of 4)


A
TEST 3 – FIND GOOD 8KW CHUNK OF PROGRAM MEMORY
FAIL?
FAULT CODE = 22 OCTAL
STATE INIT FAULT
OFF ON ON
TEST 4 – LOOK FOR LOAD DEVICE. LOAD 8 BOOT BLOCKS
FAIL?
FAULT CODE = 23 OCTAL
STATE INIT FAULT
OFF ON ON
D
OFFLINE TAPE
SYSTEM TAPE
B
B
(SYSTEM TAPE)
TURNS INIT INDICATOR OFF TURNS STATE INDICATOR ON SOLID
OUTPUTS TO TERMINAL INIPIO–I–BOOTING LOADS REST OF INIPIOC (1)
RUNS INITPIOC – WHICH INITS REQUESTORS AND GETS THEIR STATUS
FAIL?
FAULT CODE DEPENDENT ON FAILURE (2)
STATE INIT FAULT
ON OFF ON
LOADS OPERATING SOFTWARE WHILE CONTROL AND DATA MEMORY ARE TESTED BY HIGHEST NO. REQUESTOR. STATE INDICATOR BLINKS AT 1/2 SECOND INTERVALS
P.IOC TESTS REMAINDER OF PROGRAM MEMORY, AND CREATES BAD MEMORY LINKED LIST
C

NOTE 1: FIRST PORTION OF THE OFFLINE P.IOC TESTS (OFLPIO) WAS LOADED WITH THE PREVIOUS LOAD OF EIGHT BOOT BLOCKS.

NOTE 2: REFER TO FAULT CODE CHART. FOR DETAIL INFORMATION ON INITPIOC TESTS, REFER TO THE HSC50 INLINE DIAGNOSTICS USER DOCUMENTATION.

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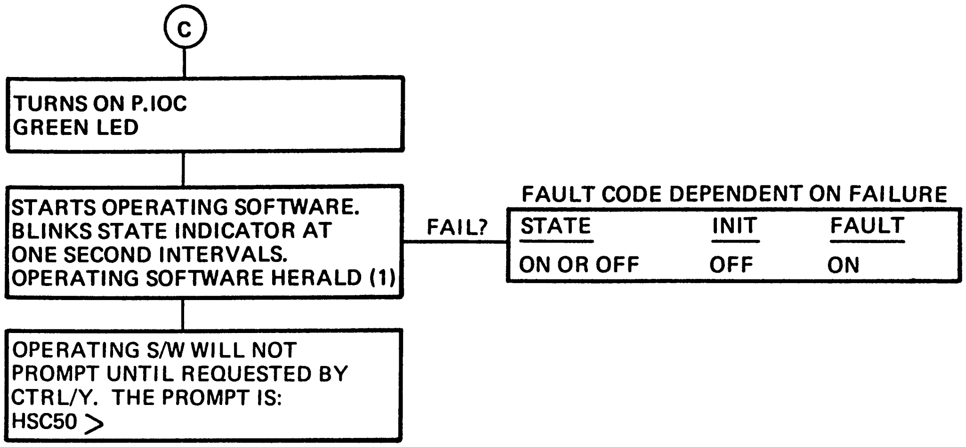
Figure 5-2 HSC50 Boot Flowchart (2 of 4)


C
TURNS ON P.IOC GREEN LED
STARTS OPERATING SOFTWARE. BLINKS STATE INDICATOR AT ONE SECOND INTERVALS. OPERATING SOFTWARE HERALD (1)
FAIL?
FAULT CODE DEPENDENT ON FAILURE
STATE
INIT
FAULT
ON OR OFF
OFF
ON
OPERATING S/W WILL NOT PROMPT UNTIL REQUESTED BY CTRL/Y. THE PROMPT IS: HSC50 >

NOTE 1: AFTER THE OPERATING SOFTWARE HERALD, ONE OF SEVERAL NONFATAL INITIALIZATION FAILURE MESSAGES MAY BE PRINTED:

– *REQUESTOR n FAILED TO INIT STATUS = XXX*

THIS MESSAGE INDICATES THE SPECIFIED REQUESTOR FAILED ITS INTERNAL INITIALIZATION SELF-TEST.

– *VC ESTABLISHED FROM HOST n*

THIS MESSAGE INDICATES THE PATH n HAS GONE FROM GOOD TO BAD. A SINGLE PATH FAILURE MAY INDICATE A BAD CI CABLE (INTERNAL OR EXTERNAL) OR LINK MODULE FAILURE IN EITHER A HOST OR THE HSC50.

– *SWAP BANK BIT SET*

THIS MESSAGE INDICATES THAT A GOOD CONTIGUOUS SECTION OF 8KW PROGRAM MEMORY COULD NOT BE FOUND WITHOUT USING THE SWAP BANK BIT IN THE P.IOC CSR. THE MEMORY MODULE MAY BE SUSPECT.

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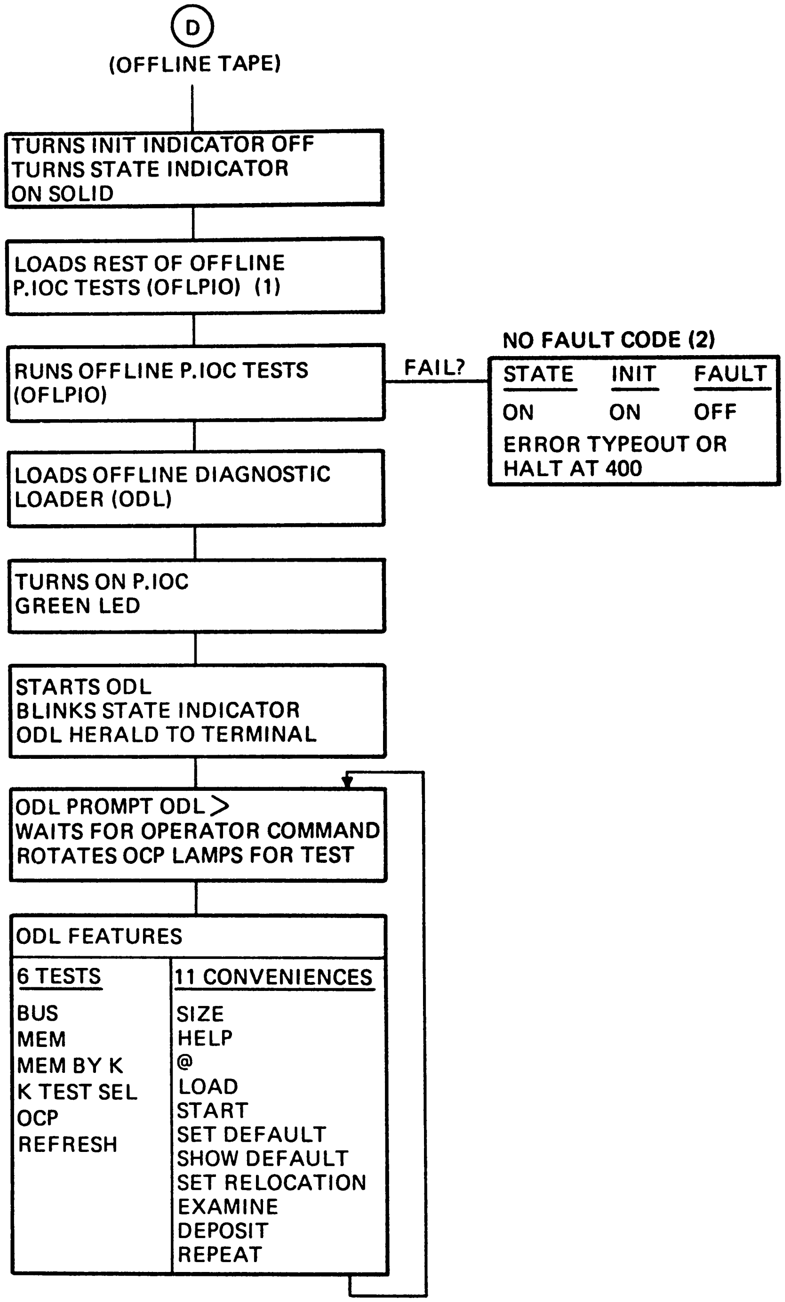
Figure 5-2 HSC50 Boot Flowchart (3 of 4)



NOTE 1: FIRST PORTION OF THE OFFLINE P.IOC TESTS (OFLPIO) WAS LOADED WITH THE PREVIOUS LOAD OF EIGHT BOOT BLOCKS.

NOTE 2: FOR DETAIL INFORMATION ON THE OFLPIO TESTS AND ERROR REPORTS, REFER TO THE HSC50 OFFLINE DIAGNOSTICS USER DOCUMENTATION.

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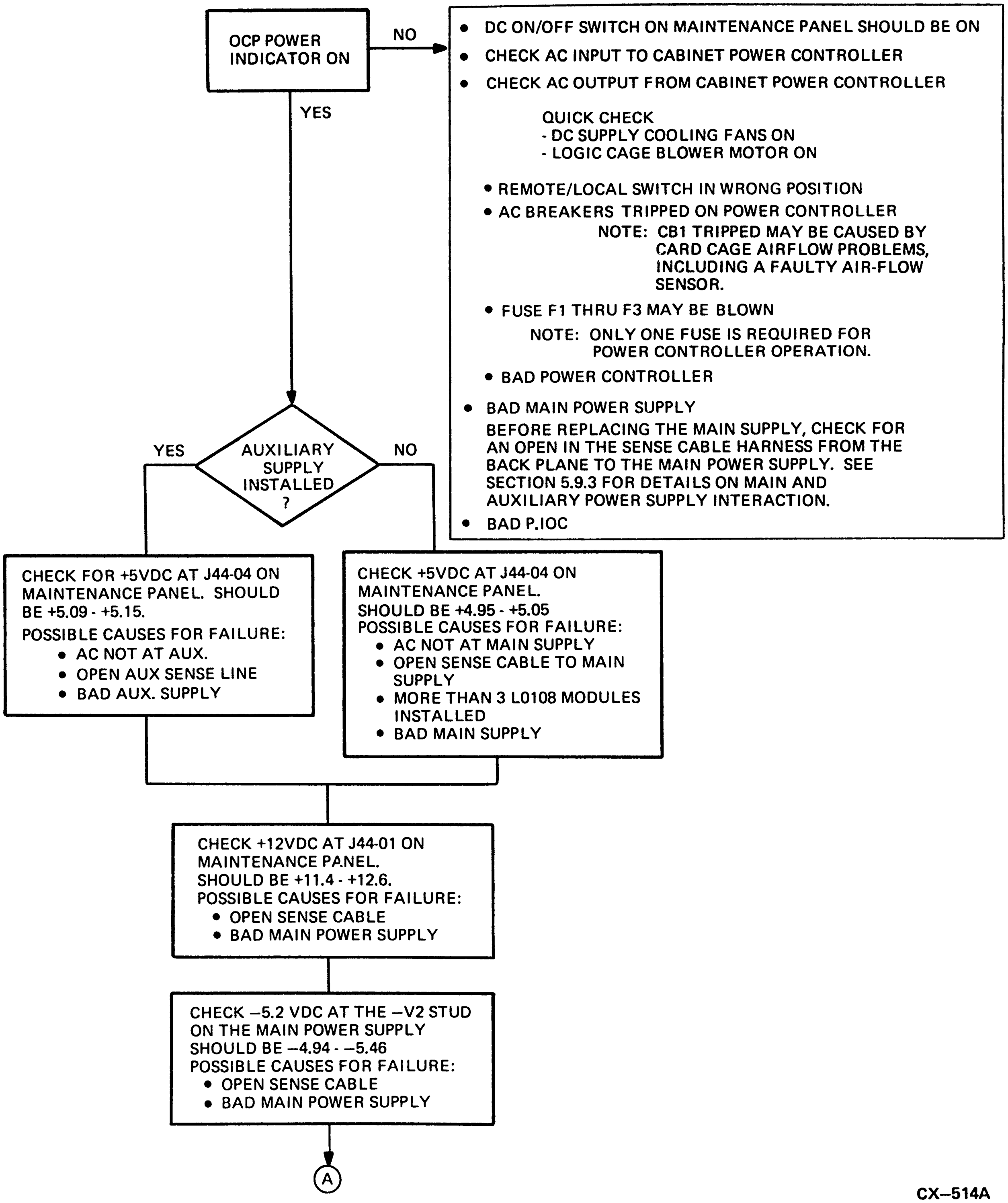
Figure 5-2 HSC50 Boot Flowchart (4 of 4)


OCP POWER INDICATOR ON
NO
YES
• DC ON/OFF SWITCH ON MAINTENANCE PANEL SHOULD BE ON
• CHECK AC INPUT TO CABINET POWER CONTROLLER
• CHECK AC OUTPUT FROM CABINET POWER CONTROLLER
QUICK CHECK
- DC SUPPLY COOLING FANS ON
- LOGIC CAGE BLOWER MOTOR ON
• REMOTE/LOCAL SWITCH IN WRONG POSITION
• AC BREAKERS TRIPPED ON POWER CONTROLLER
NOTE: CB1 TRIPPED MAY BE CAUSED BY CARD CAGE AIRFLOW PROBLEMS, INCLUDING A FAULTY AIR-FLOW SENSOR.
• FUSE F1 THRU F3 MAY BE BLOWN
NOTE: ONLY ONE FUSE IS REQUIRED FOR POWER CONTROLLER OPERATION.
• BAD POWER CONTROLLER
• BAD MAIN POWER SUPPLY
BEFORE REPLACING THE MAIN SUPPLY, CHECK FOR AN OPEN IN THE SENSE CABLE HARNESS FROM THE BACK PLANE TO THE MAIN POWER SUPPLY. SEE SECTION 5.9.3 FOR DETAILS ON MAIN AND AUXILIARY POWER SUPPLY INTERACTION.
• BAD P.IOC
AUXILIARY SUPPLY INSTALLED ?
YES
NO
CHECK FOR +5VDC AT J44-04 ON MAINTENANCE PANEL. SHOULD BE +5.09 - +5.15.
POSSIBLE CAUSES FOR FAILURE:
• AC NOT AT AUX.
• OPEN AUX SENSE LINE
• BAD AUX. SUPPLY
CHECK +5VDC AT J44-04 ON MAINTENANCE PANEL.
SHOULD BE +4.95 - +5.05
POSSIBLE CAUSES FOR FAILURE:
• AC NOT AT MAIN SUPPLY
• OPEN SENSE CABLE TO MAIN SUPPLY
• MORE THAN 3 L0108 MODULES INSTALLED
• BAD MAIN SUPPLY
CHECK +12VDC AT J44-01 ON MAINTENANCE PANEL.
SHOULD BE +11.4 - +12.6.
POSSIBLE CAUSES FOR FAILURE:
• OPEN SENSE CABLE
• BAD MAIN POWER SUPPLY
CHECK –5.2 VDC AT THE –V2 STUD ON THE MAIN POWER SUPPLY
SHOULD BE –4.94 - –5.46
POSSIBLE CAUSES FOR FAILURE:
• OPEN SENSE CABLE
• BAD MAIN POWER SUPPLY
A

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Sheet 1 of 2

Figure 5-3 Power Supply Troubleshooting Flowchart (1 of 2)

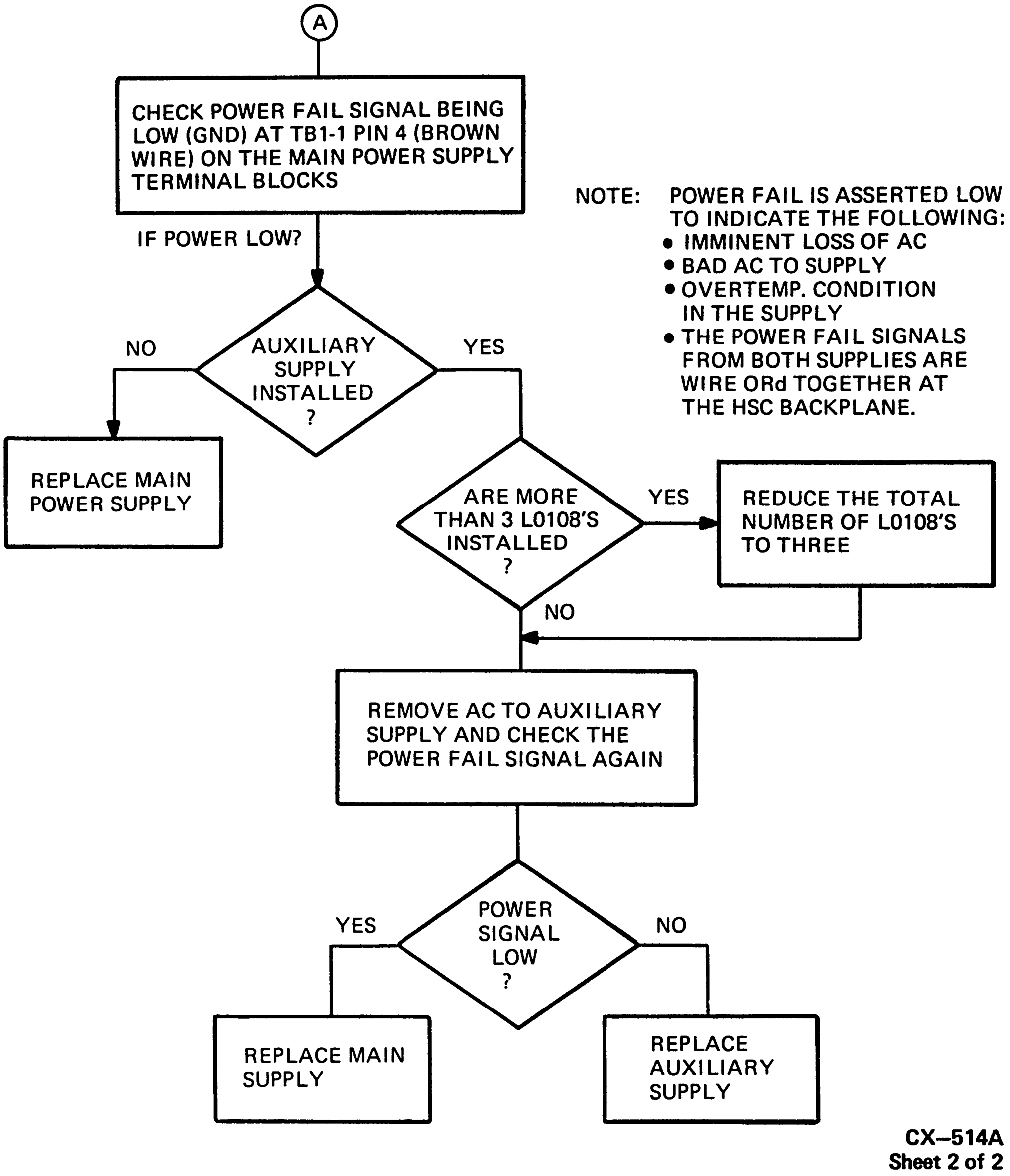
A
CHECK POWER FAIL SIGNAL BEING LOW (GND) AT TB1-1 PIN 4 (BROWN WIRE) ON THE MAIN POWER SUPPLY TERMINAL BLOCKS
IF POWER LOW?
NOTE: POWER FAIL IS ASSERTED LOW TO INDICATE THE FOLLOWING:
• IMMINENT LOSS OF AC
• BAD AC TO SUPPLY
• OVERTEMP. CONDITION IN THE SUPPLY
• THE POWER FAIL SIGNALS FROM BOTH SUPPLIES ARE WIRE ORd TOGETHER AT THE HSC BACKPLANE.
NO
AUXILIARY SUPPLY INSTALLED ?
YES
REPLACE MAIN POWER SUPPLY
ARE MORE THAN 3 L0108'S INSTALLED ?
YES
REDUCE THE TOTAL NUMBER OF L0108'S TO THREE
NO
REMOVE AC TO AUXILIARY SUPPLY AND CHECK THE POWER FAIL SIGNAL AGAIN
YES
POWER SIGNAL LOW ?
NO
REPLACE MAIN SUPPLY
REPLACE AUXILIARY SUPPLY
CX–514A
Sheet 2 of 2

Figure 5-3 Power Supply Troubleshooting Flowchart (2 of 2)

5.5 MODULE STATUS CODES

Following paragraphs discuss the module status codes and their interpretation.

5.5.1 Interpretation of Status Bytes

Status bytes interpreted in these paragraphs are for internal microdiagnostic failures detected by requestors. Such bytes displayed on the auxiliary terminal are interpreted as follows:

- **Bit 7** is the parity bit. Odd parity is used by the software. An odd status byte in bits 0 through 6 generates a clear parity bit. An even status byte generates a set parity bit.
- **Bit 6** indicates a microdiagnostic failure. With this bit set, bits 0 through 5 of the status byte indicate the test number of the failed microdiagnostic. With bit 6 clear, bits 0 through 5 indicate the module type reporting the message.
- **377** (all ones) in the status field represents no requestor present in that slot.

5.5.2 Module Type Codes

When the module successfully finishes all microdiagnostics, bit 6 of the status byte remains clear. Bits 0 through 5 of the status byte then have the following codes defining module types:

- Code 001 represents a host interface (K.ci) module set. Using odd parity, the code is reported as 001.
- Code 002 represents a disk data channel (K.sdi) module. Using odd parity, the code is reported as 002.
- Code 203 represents a tape data channel (K.sti) module. Using odd parity, the code is reported as 203.

5.6 SOFTWARE CRASH ERROR MESSAGE INTERPRETATIONS

The operating software contains numerous consistency checks. When one of these checks fails, the HSC50 performs a soft initialization sequence causing it to crash and reboot. (This sequence is similar to a CPU operating system crash due to a STOPCODE or BUGHLT.)

After the HSC50 executes the soft initialization sequence and operating software returns, a message describing the reason is displayed on the auxiliary terminal. The same message is written on the System tape where it can be examined by a SHOW EXCEPTION command.

The following paragraphs describe some of the HSC50 software crash interrupts and accompanying error examples.

5.6.1 Level 7 K Interrupt (Trap Through 134)

A Level 7 K interrupt (trap thru 134) is one of the exceptions causing the HSC50 to crash and reboot while executing functional code. This occurs when one or more requestors detect a fatal error condition. The requestor, upon detecting one of these conditions, generates a level 7 interrupt to the P.ioc. which traps thru location 134 and causes a reboot.

The error conditions detected by a requestor running functional code (not microdiagnostics) that cause a level 7 interrupt can be either microcode or hardware detected. The microcode-detected errors causing level 7 K interrupts result from a microcode consistency check failure. K.sdi hardware-detected errors are the result of errors detected on the control bus. K.ci hardware detected errors are the result of errors detected on the control bus, scratchpad RAM parity errors or data bus parity errors, and NXMs not related to a data transfer.

5.6.1.1 Control Bus Error Condition – Following are the control bus error conditions causing a level 7 K interrupt.

- CONTROL BUS ERROR – The requestor was in the process of executing a control bus cycle and received CERR L from the P.ioc. The P.ioc module sends this signal to a requestor when it detects an illegal control bus cycle type on the CCYCLE 0-2 lines.
- CONTROL BUS NXM – The requestor tried to reference control memory and did not receive an acknowledgment (CACK L) within the timeout period.
- CONTROL BUS PARITY ERROR – The requestor detected bad parity on the data it read off the control bus. (The control bus is 16 bits wide with odd byte parity.)

5.6.1.2 Requestor Status for Nonfailing Requestor – Part of the information saved in this type of crash/reboot is the status of each requestor slot. This status is printed on the HSC50 console after the reboot and is saved with the last exception reason written on the HSC50 System tape. The requestor(s) generating the level 7 interrupt are shown in the status value(s).

The following are status values returned for requestor slots that did not contain a requestor causing a level 7 interrupt. Any other requestor status value indicates the requestor in that slot detected the error and generated a level 7 interrupt.

001 – indicates the slot contains a K.ci

002 – indicates the slot contains a K.sdi

203 – indicates the slot contains a K.sti

377 – indicates the slot does not contain a requestor

5.6.1.3 Exception Codes (K.ci, K.sdi and K.sti) – Following is a list of the K.ci, K.sdi and K.sti exception codes that may be printed in the requestor status field for a failing requestor. Hardware-detected exception codes result from control bus errors; the microcode-detected exception codes result from a microcode consistency check failure. Under K.ci, the Host Clear notation means a host sent the command over the CI to cause HSC50 reinitialization (reboot). On the K.sdi and K.sti, Lower Processor Stopped indicates the lower microprocessor stopped and attempts by the upper processor to restart it failed. The leftmost two bits of the code are not shown as they have no useful meaning.

K.ci

Hardware Detected – 15,20,23,31,33-37,40-47,50,51,
53-57,60-67,70-75

Microcode Detected – 14,16,17,21,22,24-27,30,32,52,76

Host Clear – 77

K.sdi

Hardware Detected – 14,16,17,20-27,30,32-34,36,37,
40-42,44,46,47,50-55,75,76

Microcode Detected – 15,26,31,43,45

Lower Processor Stopped – 35

K.sti

Hardware Detected – 14-22,24-33,35,36,41-43,75,76

Microcode Detected – 23,37,40,74

Lower Processor Stopped – 34

Following is an example of an HSC50 console printout after a reboot caused by a level 7 K interrupt. The same information can be obtained by typing the SHOW EXCEPTION command after the HSC50 has rebooted. This command reads the last exception reason from the System tape and displays it.

```
SINI-E ERROR SEQUENCE 1. AT 03-NOV-1983 09:12:16.60
    LAST SOFT INIT CAUSED BY LEVEL 7 K INTERRUPT (TRAP THRU 134)
    FROM PROCESS DISK
    PC 046410
    STATUS OF REQUESTORS 1-4: 001 377 203 002
                5-7: 140 377 377
```

The status shown in this example indicates the following:

Requestor slot 1 contains a K.ci

Requestor slot 3 contains a K.sti

Requestor slot 4 contains a K.sdi

Requestor slots 2, 6, and 7 are empty

The requestor in slot 5 generated the level 7 interrupt. The status of 140 indicates the requestor generated the interrupt after detecting a control bus error.

Intermittent control memory, data memory, control bus and data bus problems also can cause a requestor to generate a level 7 interrupt. For this reason, replacing a module after the first occurrence of this type of failure is not recommended. Determine if the same requestor always causes the failure. If other requestors also fail, the problem may be any module on the control and data buses.

5.6.2 Parity Error (Trap through 114) Crashes

When the HSC50 is running the operating software and the P.ioc module (L0105) detects a parity error in control, data, or program memory, a trap through 114 occurs. This causes the HSC50 to crash and reboot.

When the HSC50 reboots, a message is printed on the console terminal describing the reason for the reboot. This same message is written on the HSC50 System tape where it can be examined by using the SHOW EXCEPTION command. Following is an example of the message displayed when the soft init was caused by a parity error trap (trap through 114):

```
SINI-E ERROR SEQUENCE 1. AT 17-NOV-1858 00:00:02.80
    LAST SOFT INIT CAUSED BY PARITY ERROR (TRAP THRU 114)
    FROM PROCESS PSCHED
    PC 110472
    PSW 140000
    LOW ERROR ADDR 033470
    HIGH ERROR ADDR 000001
```

The low and high error address fields contain the physical address in memory where the P.ioc detected the parity error. Current physical address ranges for the three memories are as follows:

	Address Range
Program Memory	00000000 – 00777777
Data Memory	14000000 – 14377777
Control Memory	16000000 – 16377777

During the reboot from a crash caused by a parity error trap, the failing address is first compared to the addresses on the Suspect Memory list. If none compare, the failing address is added to this list. The Suspect Memory list is eight locations long and contains addresses where the P.ioc has detected one parity or NXM error during a previous reference. If the Suspect Memory list is full, the oldest address on the list is deleted and the new address is added.

If the failing address compares to an address already on the Suspect Memory list, that address is added to the Disabled Memory list and deleted from the Suspect Memory list. The Disabled Memory list is 16 locations long, and if full, no more locations are added. The Disabled Memory list is checked by the operating software during each boot sequence. No address on this list is used again.

NOTE
The Suspect and Disabled Memory lists appearing on the System tape are not the same as the Disabled Buffer queue discussed in Section 5.6.4. The Disabled Buffer queue is built as a result of the Inline Memory diagnostic running automatically and does not survive across power failures or reboots.

Because the HSC50 operating software prevents use of locations on the Disabled Memory list, replacement of the memory module (L0106) is not necessary (or recommended) upon occurrence of an occasional parity error trap. The operating software also prevents use of faulty locations detected during the boot diagnostics. For this reason, replacement of the memory module is not necessarily a requirement when the offline diagnostics detect errors in memory.

The HSC50 memory module (L0106) does not contain any parity generating or checking circuitry. As a result, it is possible for the P.ioc or one of the requestors to write bad parity into memory. In addition, P.ioc data receivers may be failing intermittently when reading data from memory causing parity error crashes.

5.6.2.1 Error Terminology – Certain terms appear in several types of error messages. Definitions of these terms and fields are provided as follows:

- **Error flags** – A standard MSCP flag sent to the host error log. Three possible error log flags are Operation Successful (Error Flag 80), Operation Continuing (Error Flag 40), or Sequence Number Reset (Error Flag 01).
- **Recovery level** – Error recovery mechanisms specified by the drive. The drive specifies the number of levels as a drive characteristic. These levels are intended only for controller-detected data errors. They are addressed by the ERROR RECOVERY COMMAND issued by the controller when it detects unrecoverable errors. This command directs the drive to invoke a particular error recovery mechanism corresponding to the specified level.

When an unrecoverable data error occurs, an ERROR RECOVERY command is issued for the highest recovery level of that drive. This command repeats, decrementing each level, until retry is successful or it reaches level zero. The original operation is retried between each issue of the ERROR RECOVERY command.

Examples of recovery levels are: offset positive, offset negative, slew positive, etc. Actual meanings of these levels are unknown to the HSC50 which addresses drive recovery levels by number only.

- **Orig err flags** – Following is a breakdown of the bits contained in the original error flags field:

Bit No.	Mask	Definition
15	100000	ECC Error
14	040000	SERDES Overrun Error
13	020000	SDI Response/Data Line Pulse Error
12 &11	014000	Suspected Position Error – Low Header Mismatch
12	010000	Header Sync Timeout
11	004000	Header Compare Error – Compare-64 performed
10	002000	Data Sync Timeout
9	001000	Drive Clock Timeout
8	000400	SDI State Line Pulse Error
7	000200	Data Bus Overrun
6	000100	Data Memory Parity Error
5	000040	Data Memory NXM
4	000020	EDC Error
3 &2	000014	Read/Write Ready Down at End of Sector
3	000010	Lost Read/Write Ready before Transfer Begun
2	000004	Lost Receiver Ready before Transfer Begun
1	000002	Forced Error (EDC = –1)
0	000001	Drive Inoperative

These flags can also show up in the VERIFY utility when reporting an inconsistency. A printout example follows:

```
VERIFY-W-LBN 854597. HAS A CONSTANT (100020 (O)) ECC ERROR.
```

- **Recovery flags** – Flags used by the operating software in the error recovery process. A breakdown of the recovery flags field follows:

000001 – Used to indicate the LBN should be replaced.

000002 – Used to indicate the current error should be logged on the console and sent to the host, if a connection is present.

000004 – Used to indicate revectoring and replacement should be suppressed.

000010 – Used to indicate an entry for the desired LBN found in the RCT.

000020 – Used to indicate an error log message already generated for the current error.

000040 – Used to indicate the error count reported by the Inline Exerciser (ILEXER) utility should be updated.

- **Lvl A retry cnt** – The number of times Level A errors have been retried. (Level A errors are those retried by a simple retry without the drive in a special error state.)

- **Lvl B retry cnt** – The number of times Level B errors have been retried. (Level B errors are those requiring SDI intervention before retry; drive must be in a special error state.)

> **NOTE**
>
> **The basic difference between Level A and Level B errors is the SDI commands issued in the process of recovering a Level B error. In the case of a Level A error (Positioner error, Data overrun, Header sync error, or Bad header), the recovery code simply rereads the offending sector in hope that the error was transient.**
>
> **A Level B error, however, requires SDI intervention. Examples of Level B errors are: Positioner error not recoverable via Level A recovery, Drive clock dropout, State line error, response pulse error, Read/Write ready dropout during sector, SERDES overrun. A Level B positioner error has a DRIVE CLEAR command issued, a RECALIBRATE command, reseek, and then a retry. All other Level B errors have a DRIVE INIT and a DRIVE CLEAR command, then the retry.**

5.6.3 Software Inconsistency Errors

The following paragraphs describe software inconsistency errors caused by requestors timing out or by periodic diagnostic failures.

5.6.3.1 Requestors Timing Out – Requestors can be timed out by the operating software if one of the module clocks stops due to certain error detection. A message is displayed on the auxiliary terminal when the reboot is complete. This message is also written on the System tape and can be examined by executing the SHOW EXCEPTION command. Such examination determines if the software inconsistency was caused by a requestor timeout.

The process active at the time of the software inconsistency indicates which type of requestor may have been timed out by the software. The first word on the stack dump indicates whether a requestor timed out or not. Table 5-2 shows the process, the stack word, and requestor type. It is used to interpret requestor timeout problems.

> **NOTE**
>
> **All other codes in the first word on the stack indicate the software inconsistency was not caused by a requestor timing out.**

Table 5-2 Requestor Timeout

ACTIVE REQUESTOR PROCESS	SOFTWARE VERSION	FIRST WORD ON STACK	TYPE
Poller	V100	000007	K.ci
Poller	V110	000007	K.ci
Poller	V200	000007	K.ci
Disk	V100	030025	K.sdi
SDI	V110	030025	K.sdi
SDI	V200	030025	K.sdi

If the software inconsistency is caused by a K.sdi timeout, the second word on the stack should be examined. The contents of the second word are identifiers as follows:

- Low byte equals the requestor slot number
- High byte equals the active port number

5.6.3.2 Timeout Error Message Examples – Following are message examples displayed when a timeout occurs:

```
SINI-E ERROR SEQUENCE 1. AT 17-JAN-1984 00:00:16.80
    LAST SOFT INIT CAUSED BY SOFTWARE INCONSISTENCY
    FROM PROCESS POLLER
    PC 004054
    PSW 140001
    STACK DUMP: 000007 052525 052525
```

The active process indicated in the message is POLLER and 000007 is the first word on the stack. Table 5-2 indicates the cause of this inconsistency is the K.ci timing out. The most likely FRU is the L0107 (port processor) module.

```
SINI-E ERROR SEQUENCE 1. AT 11-JUN-1984 00:00:16.80
    LAST SOFT INIT CAUSED BY SOFTWARE INCONSISTENCY
    FROM PROCESS SDI
    PC 041202
    PSW 140001
    STACK DUMP: 030025 000405 000000
```

The active process indicated in this message is SDI and 030025 is the first word on the stack. Table 5-2 is used to determine if the cause of the software inconsistency is a K.sdi timing out. The low byte of the second word on the stack indicates the L0108-YA (K.sdi) module in slot 5 is the most likely cause of the failure.

5.6.3.3 Periodic Diagnostic Failures – During intervals of low activity, periodic diagnostics are scheduled to run under the HSC50 operating software. Additional information is found in Chapter 4 of this manual.

Following is a sample printout of a failure in the K.sdi module, requestor slot 2, detected by a periodic diagnostic:

```
PRKSDI>P>15:04 T#007 E#001
PRKSDI>P>K FAILED DURING DIAGNOSTIC
PRKSDI>P>REQUESTOR 2, STATUS - 307
PRKSDI>P>MICRO DIAGNOSTIC 07
```

T# equals the ROM-resident microdiagnostic that failed. The following lists the K.sdi/K.sti microdiagnostic tests:

- Test 00 indicates the Sequencer Test.
- Test 01 indicates the ALU Test.
- Test 02 indicates the Data Bus Test.
- Test 03 indicates the Control Bus Test.
- Test 04 indicates the PROM Parity Test.
- Test 05 indicates the Memory Test.
- Test 06 indicates the RAM Test.
- Test 07 indicates the SERDES/RSGEN Test.
- Test 10 indicates the Partial SDI Interface Test.

The following test numbers apply for the periodic memory diagnostic:

- Test 01 indicates the Data Memory Transceiver test.
- Test 02 indicates the Control Memory Transceiver test.
- Test 03 indicates a parity error can be forced.

E# equals one of the following errors:

- **Error 0** indicates a failure in the periodic control and data memory test.
- **Error 1** indicates the K.sdi/K.sti did not complete the microdiagnostic to be performed. An error is declared when the diagnostic takes longer than five seconds to finish.
- **Error 2** indicates the K.sdi/K.sti microcode did not return the dialog control block (DCB). The DCB is used to command the K.sdi/K.sti microcode to perform the diagnostic. A possible cause could be a control bus NXM error detected while attempting to return the DCB.

Failures in the periodic diagnostics generate an exception error, causing the HSC50 to reinitialize. The exception reason is shown on the auxiliary terminal after the reinitialization. It is also stored on the System tape and can be displayed using the SHOW EXCEPTION command.

Following is an example of an exception reason displayed after a reinitialization:

```
SINI-E ERROR SEQUENCE 1. AT 17-NOV-1858  00:00:02.80
    LAST SOFT INIT CAUSED BY SOFTWARE INCONSISTENCY
    FROM PROCSS PDEMON
    PC  113606
    PSW 140000
    STACK DUMP: 000004 104030 140310
```

This diagnostic message identifies PDEMON as the currently running process and indicates the stack dump display contains no useful information. The periodic diagnostic failure printout must be examined to determine which requestor failed. Following is an example of a message displayed when a K.sdi also failed on the reboot:

```
SINI-E ERROR SEQUENCE 2. AT 17-NOV-1858 00:00:02.80
     REQUESTOR 2 FAILED INIT DIAGS, STATUS - 107
```

5.6.4 REQUESTOR-DETECTED DATA MEMORY ERRORS

If one of the requestors detects a parity error or NXM error while referencing data memory, the following events occur:

- The address of the buffer causing the error is sent to a special queue to be tested.
- The data transfer is retried using another buffer.
- The inline memory diagnostic is scheduled to test the failing buffer.

Buffers failing the memory test are sent to the Disabled Buffer queue and are not used again. Buffers passing the memory test are returned to the Free Buffer queue and are available for use. Addresses of those buffers passing the memory test are saved to determine later if a buffer is sent a second time for testing. If a buffer is queued for testing a second time, it is added automatically to the Disabled Buffer queue.

An MSCP error message with an event code of 012A is sent to the host and logged in the system error log. An error message and output from the Inline Memory (ILMEMY) test are also printed on the auxiliary terminal. When an error referencing data memory is detected, the error message and output from ILMEMY are displayed on the terminal.

In the following output example, ILMEMY did not detect a failure when testing the buffer. This error output example contains several HSC50-specific terms. They are defined in section 5.6.2.1.

```
ERROR-E DATA MEMORY ERROR (NXM OR PARITY) AT 2-FEB-1984 11:01:57.37
     COMMAND REF          EFA9000F
     RA81 UNIT            7.
     ERR SEQ              1.
     ERROR FLAGS          01
     EVENT                012A
     RECOVERY LEVEL       0.
     RECOVERY COUNT       1.
     LBN                  380.
     ORIG ERR FLAGS       000040
     RECOVERY FLAGS       000002
     LVL A RETRY CNT      0.
     LVL B RETRY CNT      0.
     BUFFER ADDR          140644
     SOURCE REQ.          3.
     DETECTING REQ.       3.
ERROR-I END OF ERROR

ILMEMY>A>11:03 EXECUTION STARTING

ILMEMY>A>11:03 T#001 E#001
ILMEMY>A>RETURNED BUFFER TO FREE BUFFER LIST
ILMEMY>A>FRU1-M.STD FRU2-
ILMEMY>A>BUFFER STARTING ADDRESS (PHYSICAL) - 14064400
ILMEMY>A>BUFFER ENDING ADDRESS (PHYSICAL) - 14065476
ILMEMY>A>11:03 EXECUTION COMPLETE
```

5.7 MSCP EVENT CODES

The following paragraphs describe status and event codes displayed as a result of a subsystem problem. Tables 5-3 through 5-9 can be used for code interpretation in problem analysis.

Table 5-3 Major MSCP Status and Event Codes

Value Dec.	Oct.	Hex.	Status or Event Code
31	37	1F	Status/event code mask
32	40	20	Subcode multiplier
0	0	0	Success
1	1	1	Invalid command
2	2	2	Command aborted
3	3	3	Unit offline
4	4	4	Unit available
5	5	5	Media format error
6	6	6	Write protected
7	7	7	Compare error
8	10	8	Data error
9	11	9	Host buffer access error
10	12	A	Controller error
11	13	B	Drive error
31	37	1F	Message from an internal diagnostic

5.7.1 Notes for Tables 5-4 through 5-9

- The combination of a status or event code with a subcode is expressed as follows (assuming 16-bit symbols):

```
(SUBCODE*ST.SUB)+CODE
```

- The standard subcode values (Table 5-4) are only returned as status codes in End messages. They are never returned as event codes in Error Log messages.
- The nonstandard subcode values (Tables 5-5 through 5-9) may be returned as both status codes and event codes. In those tables, an asterisk in the EV column indicates the code and subcode may be returned as an event code. An asterisk in the ST column indicates the code and subcode may be returned as a status code.
- The letters to the right of the subcode tables indicate which controller implements that subcode. The letter U indicates UDA50A and the letter H indicates the HSC50. An uppercase letter indicates the controller fully implements the subcode; a lowercase letter indicates the controller partially implements the subcode.

Table 5-4 Standard Status Subcode Values

Sub-code	Code + Subcode Dec.	Oct.	Hex.	Status Subcode	
Success subcode values:					
0	0	0	0	Normal	UH
1	32	40	20	Spindown ignored	UH
2	64	100	40	Still connected	UH
4	128	200	80	Duplicate unit number	UH
8	256	400	100	Already online	UH
16	512	1000	200	Still online	H

(Cont.)

Table 5-4 Standard Status Subcode Values

Sub-code	Code + Subcode Dec.	 Oct.	 Hex.	Status Subcode	
Invalid Command subcode values:					
0	1	1	1	Invalid message length	UH
Many				Other invalid command subcode values should be referenced as follows. Note, this is combined with the status code: offset*256.+code Offset is the command message offset symbol for the field in error and code is the symbol for the Invalid Command status code.	UH
Command Aborted subcode values:					
0	2	2	2	Subcodes are not used.	UH
Unit Offline subcode values:					
0	3	3	3	Unit unknown or online to another controller.	UH
1	35	43	23	No volume mounted or drive disabled via RUN/STOP switch (unit is in known substate).	UH
2	67	103	43	Unit is inoperative. For SI drives, the controller has marked the drive inopera tive due to an unrecoverable error in a previous level 2 exchange, the drive C1 flag is set, or the drive has a duplicate unit identifier.	UH
4	131	203	83	Duplicate unit number	UH
8	259	403	103	Unit disabled by field service or diagnostic. For SI drives, the drive DD flag is set.	UH
Unit Available subcode values:					
0	4	4	4	Subcodes are not used.	UH
Media Format Error subcode values – refer to Table 5-5.					
Write Protected subcode values:					
256	8198	20006	2006	Unit is hardware write protected.	UH
128	4102	10006	1006	Unit is software write protected.	U

(Cont.)

Table 5-4 Standard Status Subcode Values

Sub-code	Code + Subcode			Status Subcode	
	Dec.	Oct.	Hex.		
Compare Error subcode values:					
0	7	7	7	Subcodes are not used.	
Data Error subcode values – refer also to Table 5-6.					
0	8	10	8	Sector was written with Force Error modifier.	UH
Host Buffer Access Error subcode values – refer to Table 5-7.					
Controller Error subcode values – refer also to Table 5-8.					
0	10	12	A	Reserved for host command timeout expired.	
Drive Error subcode values – refer to Table 5-9.					

Table 5-5 Media Format Error Subcode Values

Sub-code	Code + Subcode			EV	ST	Status or Event Subcode	
	Dec.	Oct.	Hex.				
Many				*	*	Data Error accessing RCT or FCT.	UH
For every Data Error subcode that may be reported as a status code, the same subcode value may be returned as a Media Format Error subcode value. Each subcode listed in Table 5-6 with an asterisk in the ST column indicates a transfer to the unit FCT or RCT. The subcode reports the error that occurred on the last copy of the multicopy structure. For example, the subcode value 7 (combined code and subcode value, 229 decimal) indicates the FCT or RCT is unreadable due to an Uncorrectable ECC Error.							
The following subcode values also exist:							
5	165	245	A5		*	Disk not formatted with 512-byte sectors. The disk FCT indicates it is formatted with 576-byte sectors, although both the controller and the drive support only 512-byte sectors.	UH
6	197	305	C5		*	Disk not formatted or FCT corrupted. The disk FCT indicates the disk is not formatted in either 512- or 576-byte mode.	UH

(Cont.)

Table 5-5 Media Format Error Subcode Values

Sub-	Code + Subcode			E	S		
code	Dec.	Oct.	Hex.	V	T	Status or Event Subcode	
8	261	405	105	*9	*	RCT corrupted. The RCT search algorithm encountered an invalid RCT entry. The subcode may be returned under the following conditions: during replacement of a block, revectoring a faulty block, and when a unit is brought online.	H
9	293	445	125	*		No replacement block available. Replacement of a faulty block was attempted but a replacement block could not be allocated (i.e. the RCT is full). This subcode may be returned during actual replacement and when an interrupted replacement is completed as part of bringing a unit online.	H

Table 5-6 Data Error Subcode Values

Sub-	Code + Subcode			E	S		
code	Dec.	Oct.	Hex.	V	T	Status or Event Subcode	
0	8	10	8		*	Sector was written with Force Error modifier.	UH
2	72	110	48	*	*	Invalid header The subsystem read an invalid or inconsistent header for the requested sector. For recoverable errors, this code implies a retry of the transfer read a valid header. For unrecoverable errors, this code implies the subsystem attempted tertiary revectoring and determined the requested sector is not revectored. Causes of an invalid header include header missync, header sync timeout, and an unreadable header.	UH
3	104	150	68	*	*	Data Sync not found (Data Sync timeout).	UH

(Cont.)

Table 5-6 Data Error Subcode Values

Sub-	Code + Subcode			E	S		
code	Dec.	Oct.	Hex.	V	T	Status or Event Subcode	
4	136	210	88	*		Correctable error in ECC field. A transfer encountered a correctable error where only the ECC field was affected. All data bits were correct but a portion of the ECC field was incorrect. The severity of the error (the number of symbols in error) is unknown. If the number of symbols in error is known, an n Symbol ECC Error subcode should be returned instead.	
7	232	350	E8	*	*	Uncorrectable ECC Error A transfer without the Suppress Error Correction modifier encountered an ECC error exceeding the correction capability of the subsystem error correction algorithms or a transfer with the Suppress Error Correction modifier encountered an ECC error of any severity.	UH
8	264	410	108	*		One-Symbol ECC Error.	UH
9	296	450	128	*		Two-Symbol ECC Error.	UH
10	328	510	148	*		Three-Symbol ECC Error.	UH
11	360	550	168	*		Four-Symbol ECC Error.	UH
12	392	610	188	*		Five-Symbol ECC Error.	UH
13	424	650	1A8	*		Six-Symbol ECC Error.	UH
14	456	710	1C8	*		Seven-Symbol ECC Error.	UH
15	488	750	1E8	*		Eight-Symbol ECC Error. A transfer encountered a correctable ECC error with the specified number of ECC symbols in error. The number of symbols in error roughly corresponds to the severity of the error.	UH

Table 5-7 Host Buffer Access Error Subcode Values

Sub-code	Code + Subcode Dec.	Oct.	Hex.	E V	S T	Status or Event Subcode	
0	9	11	9		*	Host buffer access error; cause not available. The controller was unable to access a host buffer to perform a transfer, but has no visibility into the cause of the error.	H
1	41	519	29		*	Odd transfer address.	U
2	73	111	49		*	Odd byte count.	U
3	105	151	69		*	Nonexistent memory error.	U
4	137	211	89		*	memory parity error.	U

Table 5-8 HSC50 Error Subcode Values

Sub-code	Code + Subcode Dec.	Oct.	Hex.	E V	S T	Status or Event Subcode	
0	10	12	A	*	*	Reserved for host; command timeout expired.	
1	42	52	2A	*	*	SERDES overrun or underrun error. Either the drive is too fast for the controller or a controller hardware fault has prevented controller microcode from being able to keep up with data transfer to or from the drive.	UH
2	74	112	4A	*	*	EDC Error The sector was read with correct or correctable ECC and an invalid EDC. A fault probably exists in the ECC logic of either this controller or the controller that last wrote the sector.	UH
3	106	152	6A	*	*	Inconsistent internal control structure. A high-level check detected an inconsistent data structure. For example, a reserved field contained a nonzero value or the value in a field was outside its valid range. This error almost always implies the existence of a microcode problem.	UH

(Cont.)

Table 5-8 HSC50 Error Subcode Values

Sub-code	Code + Subcode			EV	ST	Status or Event Subcode	
	Dec.	Oct.	Hex.				
4	138	212	8A	*	*	Internal EDC error A low-level check detected an inconsistent data structure. For example, a microcode-implemented checksum or vertical parity (hardware parity is horizontal) associated with internal sector data was inconsistent. This error usually implies a fault in the memory addressing logic of one or more controller processing elements. It can also result from a double bit error or other error exceeding the error detection capability of the controller hardware memory checking circuitry.	H H H
8	266	412	10A	*	*	Controller overrun or underrrun The controller attempted to perform too many concurrent transfers, causing one or more of them to fail due to a data overrun or underrun.	
9	298	452	12A	*	*	Controller memory error The controller detected an error in an internal memory, such as a parity error or nonresponding address. This subcode applies only to errors not affecting the ability of the HSC50 to properly generate End and Error Log messages. Errors affecting End and Error Log messages are not reported via MSCP. For most controllers, this subcode is returned only for controller memory errors in data or buffer memory and noncritical control structures. If the controller has several such memories, the specific memory involved is reported as part of the error address in the error log message.	
10	330	512	14A	*		PLI reception buffer parity error	
11	362	552	16A	*		PLI transmission buffer parity error	

Table 5-9 Drive Error Subcode Values

Sub-code	Code + Subcode			E V	S T	Status or Event Subcode	
	Dec.	Oct.	Hex.				
1	43	53	2B	*	*	Drive command timeout For SI drives, the controller timeout expired for either a Level 2 exchange or the assertion of Read/Write Ready after an Initiate Seek.	UH
2	75	113	4B	*	*	Controller-detected transmission error. For SI drives, the controller detected an invalid framing code or a checksum error in a Level 2 response from the drive. The UDA50A also returns this subcode for controller-detected protocol errors. All other SI controllers return subcode 9 for protocol errors.	UH
3	107	153	6B	*	*	Positioner error (misseek) The drive reported a seek operation was successful but the controller determined the drive had positioned itself to an incorrect cylinder.	UH
4	139	213	8B	*	*	Lost Read/Write Ready during or between transfers. For SI drives, Read/Write Ready drops when the controller attempts to initiate a transfer or at the completion of a transfer with Read/Write Ready previously asserted. This usually results from a drive-detected transfer error, where additional error log messages containing the drive-detected error subcode may be generated.	UH
5	171	253	AB	*	*	Drive clock dropout For SI drives, either data or state clock was missing when it should have been present. This is usually detected by means of a timeout.	UH

(Cont.)

Table 5-9 Drive Error Subcode Values

Sub-code	Code + Subcode			EV	ST	Status or Event Subcode	
	Dec.	Oct.	Hex.				
6	203	313	CB	*	*	Lost receiver ready for transfer. For SI drives, Receiver Ready was negated when the controller attempted to initiate a transfer or did not assert at the completion of a transfer. This includes all cases of the controller timeout expiring for a transfer operation (Level 1 real time command).	UH
7	235	353	EB	*	*	Drive-detected error For SI drives, the controller received a Get Status or unsuccessful response with EL set or the controller received a reponse with the DR flag set and it does not support automatic diagnosis for that drive type.	UH
8	267	413	10B	*	*	Controller-detected pulse or state parity error For SI drives, the controller detected a pulse error on either the state or data line or the controller detected a parity error in a state frame.	UH
9	299	453	12B			Drive-requested error log (EL bit set)	H
10	331	513	14B	*	*	Controller-detected protocol error For SI drives, a Level 2 response from the drive had correct framing codes and checksum but was not a valid response within the constraints of the SI protocol. The response had an invalid opcode, was an improper length or was not a possible response in the context of the exchange.	H
11	363	553	16B	*	*	Drive failed initialization For SI drives, the drive clock did not resume following a controller attempt to initialize the drive. This implies the drive encountered a fatal initialization error.	H

(Cont.)

Table 5-9 Drive Error Subcode Values

Sub-code	Code + Subcode Dec.	Oct.	Hex.	E V	S T	Status or Event Subcode	
12	395	613	18B	*	*	Drive ignored initialization For SI drives, the drive clock did not cease following a controller attempt to initialize the drive. This implies the drive did not recognize the initialization attempt.	H
13	427	653	1AB	*	*	Receiver Ready collision For SI drives, the controller attempted to assert its Receiver Ready when the Receiver Ready of the drive was still asserted.	H
14	459	713	1CB	*		Response overflow A drive sent back more frames than the reception buffer could hold. This can be caused by a hung drive microdiagnostic or a malfunctioning K.sdi.	H

5.8 TMSCP EVENT CODES

Table 5-10 lists the major TMSCP event codes. These codes are a subset of MSCP and are specific only to tape. Some of the codes in MSCP also apply to tape. Tables 5-11 through 5-15 describe TMSCP error codes and can be used for problem analysis.

Table 5-10 Major TMSCP Status and Event Codes

Hex. Value	Status or Event Code
1F	Status/event code mask
32	Subcode multiplier
0	Success
1	Invalid command
2	Command aborted
3	Unit offline
4	Unit available
5	Media format error
6	Write protected
7	Compare error
8	Data error
9	Host buffer access error
A	Controller error
B	Drive error
C	Formatter error
11	Position lost error

Table 5-11 Data Errors – Major Code 08

Code	Subcode	Major Code + Subcode	Description
−1	7FF	FFE8	Host requested retry suppression on a formatter-detected error.
−2	7FE	FFC8	Reverse retry currently not supported.
−3	7FD	FFA8	Host requested retry suppression on a K.sti-detected error.
−4	7FC	FF88	Controller transfer retry limit exceeded.
−5	7FB	FF68	Formatter retry sequence exhausted.

Table 5-12 Controller Errors – Major Code 0A

Code	Subcode	Major Code + Subcode	Description
−03	7FD	FFAA	Data overflow due to Pipeline error – No data buffers in HSC50 data memory were available when the K.sti needed one during a data transfer.
−04	7FC	FF8A	Buffer EDC error – The K.sti detected an EDC error on the data buffer it read from memory on a Write operation.
−05	7FB	FF6A	Lower processor error – A bit was set in the lower processor error register. Bits included in the lower processor error register are Data Bus NXM, Data Serdes Overrun Data Bus Overrun, Data Bus Par Err, Data Pulse Missing, and Sync Real Time Par Err.
−12	7F4	FE8A	Lower processor timeout – The upper processor in the K.sti detected the lower processor had stopped and restarted it.
−15	7F1	FE2A	Record EDC error – On a read from tape operation the EDC calculated by the K.sti did not match the EDC generated by the tape formatter.
−21	7EB	FD6A	ACKNOWLEDGE not asserted at start of transfer – The HSC50 is ready to start a transfer by sending the formatter a Level 1 command and the formatter does not have ACKNOWLEDGE asserted.

(Cont.)

Table 5-12 Controller Errors – Major Code 0A

Code	Subcode	Major Code + Subcode	Description
−23	7E9	FD2A	DATA READY timeout – This controller did not detect DATA READY from the formatter within 5 ms after sending it a Level 1 command.
−25	7E7	FCEA	RECEIVER READY not asserted at start of transfer – The HSC50 is ready to start a transfer by sending the formatter a Level 1 command and the formatter does not have RECEIVER READY asserted.
−27	7E5	FCAA	Word Rate Clock timeout – The K.sti detected the loss of clocks from a drive during a transfer.
−99	79D	F3AA	Unknown K.tape error

Table 5-13 Drive Errors – Major Code 0B

Code	Subcode	Major Code + Subcode	Description
−1	7FF	FFEB	Cannot clear drive errors.
−2	7FE	FFCB	Could not position for (formatter) retry.
−5	7FB	FF6B	Tape drive requested error log.
−10	7F8	FF0B	ERASE command failed.
−11	7F7	FEEB	ERASE GAP command failed.
−12	7F6	FECB	Could not complete online sequence.
−13	7F5	FEAB	Rewind failure.
−14	7F4	FE8B	Unable to position to before LEOT.
−15	7F3	FE6B	Could not set unit characteristics.
−16	7F2	FE4B	Could not write tape mark.
−17	7F1	FE2B	Could not set byte count.

Table 5-14 Formatter Errors – Major Code 0C

Code	Subcode	Major Code + Subcode	Description
−1	7FF	FFEC	Could not get formatter summary status during transfer error recovery.
−2	7FE	FFCC	Cannot clear formatter errors.
−5	7FB	FF6C	Formatter requested error log.
−10	7F8	FF0C	TOPOLOGY command failed.
−20	7F0	FE0C	Could not get formatter summary status while trying to restore tape position.
−21	7EF	FDEC	Could not get extended drive status.

Table 5-15 Position Lost Errors – Major Code 11

Code	Subcode	Major Code + Subcode	Description
−1	7FF	FFF1	Controller-detected position lost.
−2	7FE	FFD1	Formatter and HSC50 disagree on tape position.
−5	7FB	FF71	Formatter-detected position lost.
−7	7F9	FF31	Retry limit exceeded while attempting to restore tape position.

5.9 POWER SYSTEM

Figures 5-4 through 5-7 show voltage test points for the maintenance panel, the main and auxiliary power supplies, and the airflow sensor. Figures 5-5 and 5-7 are especially helpful in checking the POWER FAIL signal.

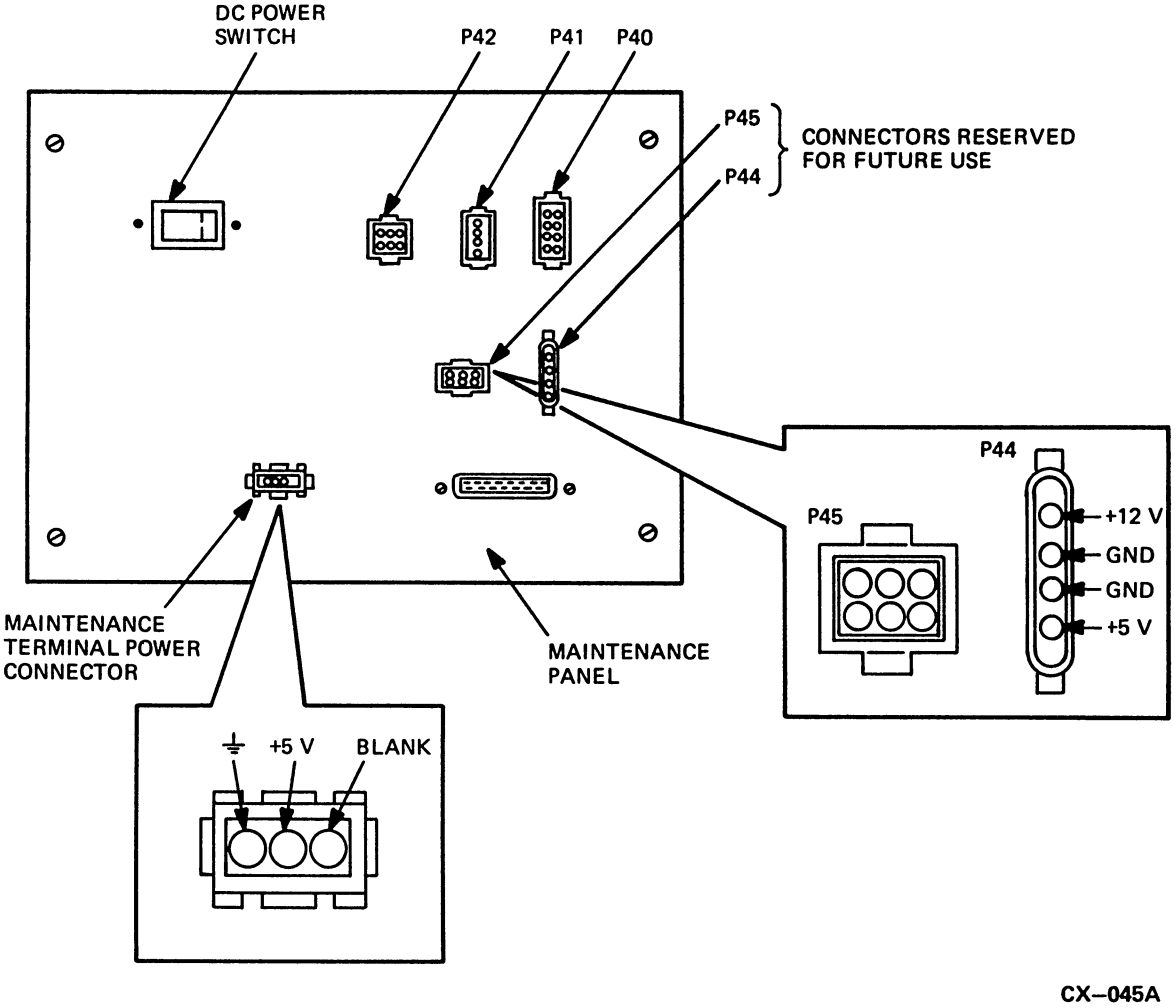

Figure 5-4 Maintenance Panel Test Points

5.9.1 POWER FAIL Signal

This signal indicates the imminent loss of dc voltage due to ac power loss or to internal thermal shutdown. Either the main or the auxiliary power supply can generate this signal which is asserted low (GND). POWER FAIL is checked at the following power supply locations:

- Main power supply – TB1-2 (4) (Refer to Figure 5-5.)
- Auxiliary power supply – TB1 (4) (Refer to Figure 5-7.)

When this signal is detected by the F11 chip set on the I/O Control Processor, the HSC50 executes a power fail routine. Although one of the power supplies outputs the POWER FAIL signal, it is not an input to the other. Therefore, one supply can be generating the signal while the other continues to output voltages. For this reason, both power supplies must be checked for POWER FAIL low (GND) when the power system is suspect.

Note also the POWER FAIL signal is not an input to the Power indicator on the Operator Control Panel (refer to section 2.2.3). If the auxiliary power supply is generating POWER FAIL, the Power indicator probably is still illuminated.

WIRE LIST					
COLOR	POSITION	SIGNAL	COLOR	POSITION	SIGNAL
PUR	TBI-3-5	12 V	PUR	TBI-3-1	12 V SENSE
PUR	TBI-3-6	12 V	BLU	TBI-2-7	ACC
BLK	TBI-3-3	GND (12 V)	BRN	TBI-2-6	AC
BLK			GRN/YEL	TBI-2-5	GND
ORN	TBI-2-2	–5 V SENSE	YEL	TBI-2-3	ON/OFF (–5, 3 V)
BLK	TBI-2-1	GND (–5 V SENSE)	ORN	TBI-2-2	–5 V SENSE (S2–)
BRN	TBI-1-4	POWER FAIL	BLU	TBI-1-3	ON/OFF 5 V
BLK	TBI-1-2	GND (5 V SENSE)	BLK	TBI-1-2	GND (5 V SENSE)
RED	TBI-1-1	5 V SENSE	PUR	TBI-3-2	12 V
BLK	TBI-3-4	GND (12 V SENSE)			

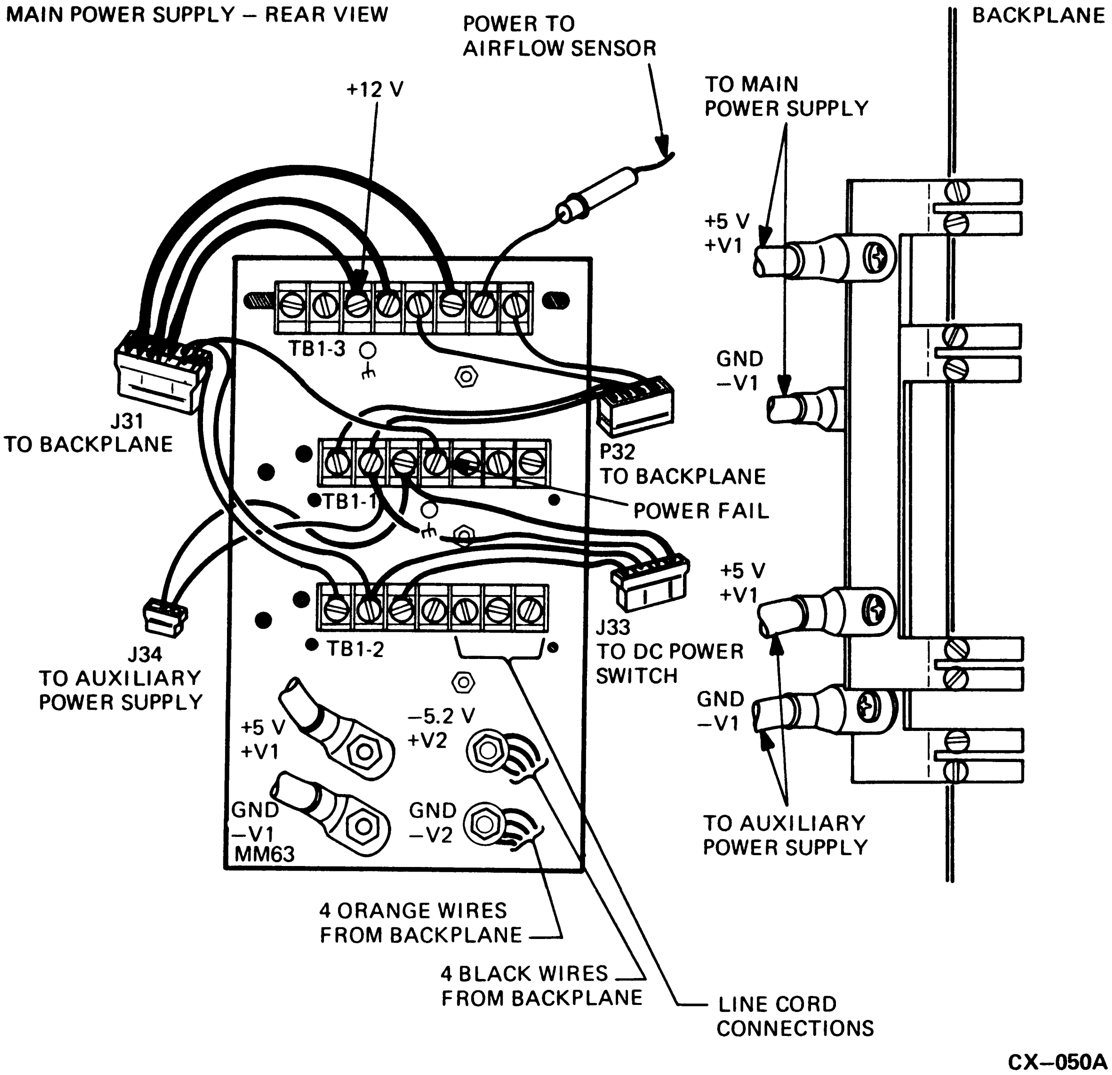

Figure 5-5 Main Power Supply Test Points

5.9.2 Airflow Sensor

Test points for the airflow sensor are shown in Figure 5-6. The sensor is physically located in the exhaust duct at the rear of the cabinet. A power source of −5.2 volts from the backplane to +12 volts on the main power supply heats the sensor. When the cooling system is working properly, the temperature of the sensor is lowered. If the blower fails or the exhaust is too hot, the sensor pulls relay K1 through the same power source. This trips the main circuit breaker (CB1) on the AC Power Controller.

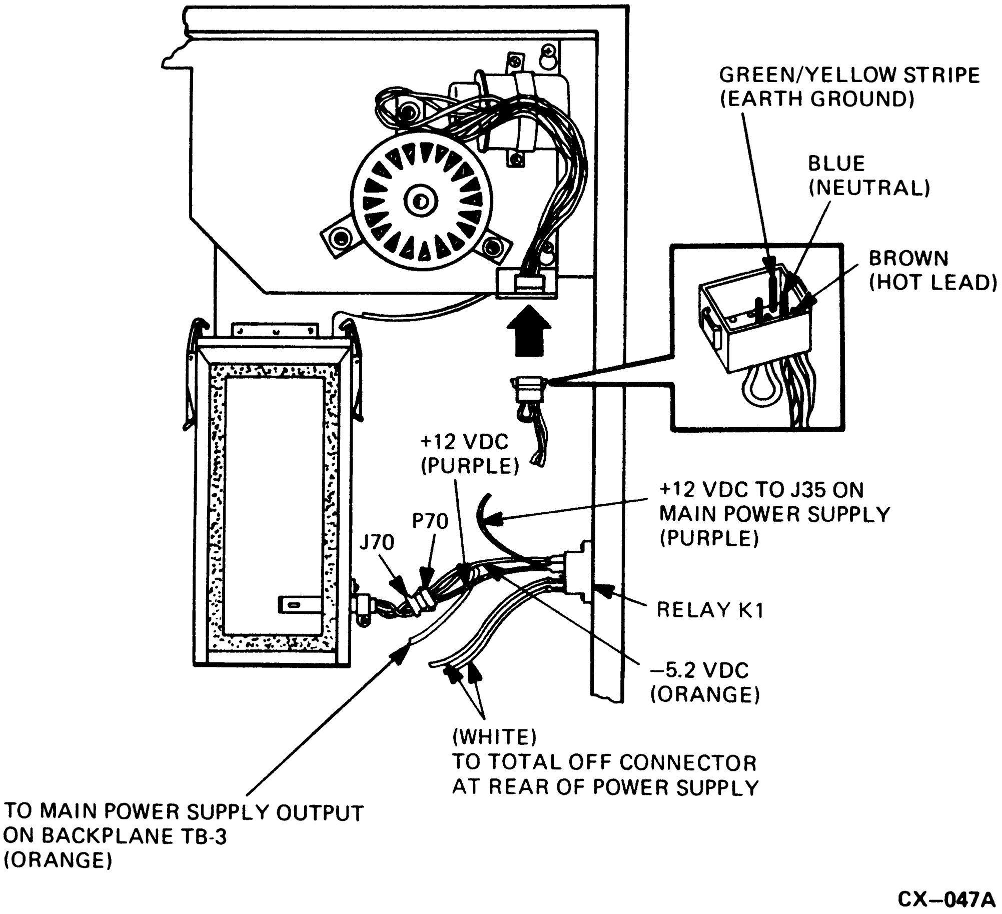

Figure 5-6 Airflow Sensor Test Points

WIRE LIST		
COLOR	POSITION	SIGNAL
BLACK	TBI-2	GROUND (5 V SENSE)
RED	TBI-1	5 V SENSE
BROWN	TBI-4	POWER FAIL
BLUE	TBI-7	ACC
BROWN	TBI-6	AC
GRN/YEL	TBI-5	CHASSIS GROUND
BLUE	TBI-3	ON/OFF
BLACK	TBI-2	GROUND (5 V SENSE)

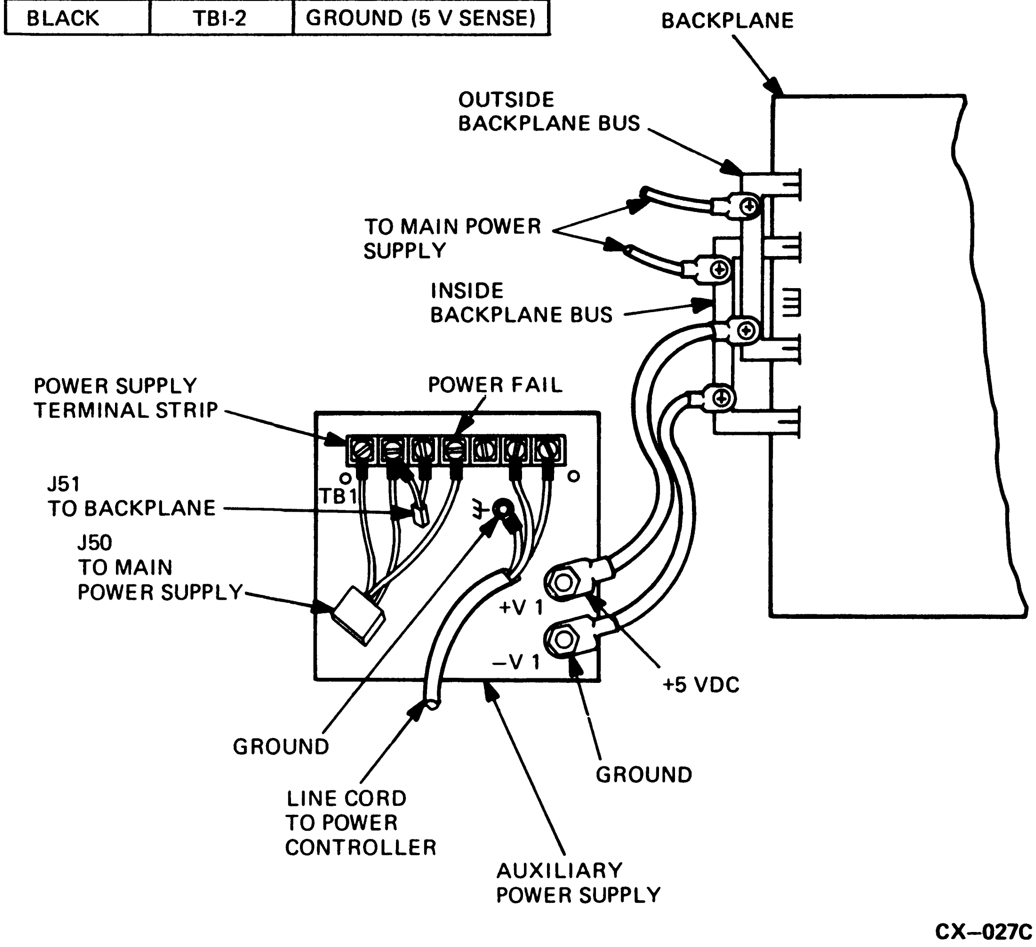

Figure 5-7 Auxiliary Power Supply Test Points

5.9.3 Main/Auxiliary Power Supply Interaction

In configurations with more than three data channels, an auxiliary power supply must be installed. Certain interaction then occurs between the two supplies.

Both the main and the auxiliary power supplies generate +5 volts; in addition, the main power supply generates +12 and −5.2 volts. Depending on whether an auxiliary power supply is present, the main power supply operates in one of two modes as follows:

	+5 Volt	−5.2 Volts	+12 Volts
No Auxiliary Supply	100 A	35 A	2 A
With Auxiliary Supply	65 A	70 A	2 A

The auxiliary power supply can provide 135 amps and is adjusted to 5.1 volts.

In an HSC50 with two power supplies, the +5 volt output of both supplies is tied together at a bus bar on the backplane. The auxiliary power supply generates +5 volts until the load exceeds 135 amps. At this point, the auxiliary supply goes into current foldback causing its voltage to drop. The main power supply senses this voltage drop over sense lines connected to the HSC50 backplane. When it senses the voltage has dropped to +5.0 volts, the main supply also begins supplying +5 volts. Together the main and auxiliary power supply can produce up to 200 amps of +5 volts.

The voltage measured at the maintenance access panel on an HSC50 containing **both** the main and auxiliary power supplies should be +5.1 volts and not +5.0 volts. If +5.0 volts is measured there when **both** supplies are installed, the auxiliary supply is probably not working. This can be verified by disconnecting ac power to the main supply and measuring the +5 volts again. If the +5 volts does not measure +5.1, the auxiliary power supply should be replaced.

5.10 HSC50 INTERNAL CABLING

Figure 5-8 diagrams the internal HSC50 cabling.

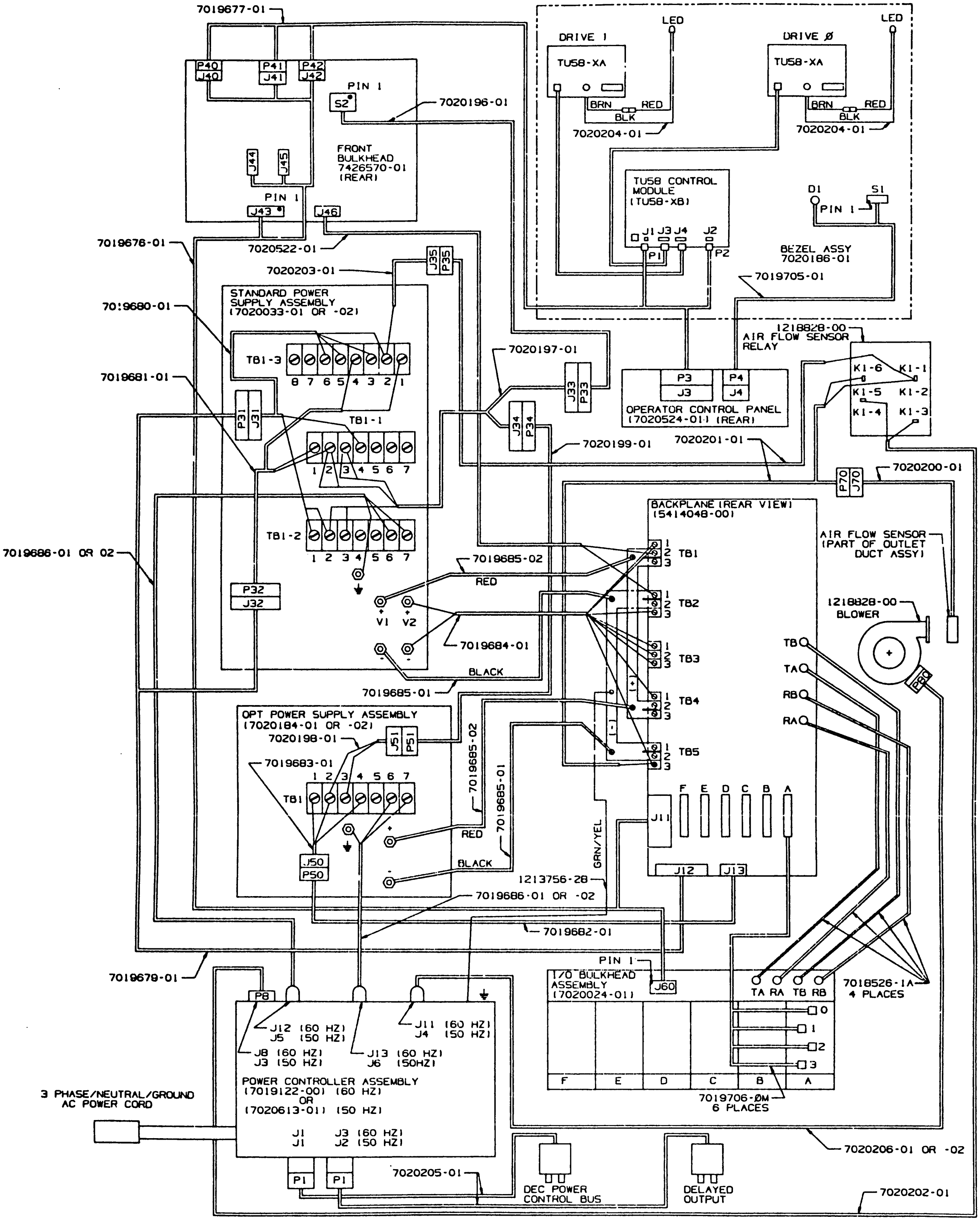

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Figure 5-8 HSC50 Internal Cabling (1 of 5)

WIRE TABLE FOR LINE CORD OF 7019122-00			
COLOR	FROM	TO	REMARKS
BLUE	W	LF1-N	LINE SIDE
BLACK	Z	LF1-L3	
GRN/YEL	GND	LF1-GND	
BLACK	Y	LF1-L2	
BROWN	X	LF1-L1	

WIRE TABLE FOR 7019676-01				
COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	J11-1	J41-01	+12V	• PINS AT J43-06 AND J60-06 ARE WIRELESS PINS. THEY ARE TIED TO J43-20 AND J60-20 BY COMMONING STRIPS.
VIOLET	J11-2	J44-01	+12V	
BLACK	J11-3	J41-02	GROUND	
BLACK	J11-4	J41-03	GROUND	
BLACK	J11-5	J44-02	GROUND	
BLACK	J11-6	J44-03	GROUND	
RED	J11-7	J41-04	+5V	
RED	J11-8	J44-04	+5V	
WHITE	J11-12	J60-20	TERM PRES L	
WHITE	J11-13	J60-01	XMT-	
WHITE	J11-14	J60-02	XMT+	
WHITE	J11-15	J60-03	RCV+	
-/——/-	J60-20	J60-06	DATA SET READY COMMONING STRIP SEE NOTE •	
WHITE	J11-16	J60-07	RCV-	
WHITE	J11-18	J43-20	TERM PRES L	
WHITE	J11-19	J43-01	XMT-	
WHITE	J11-20	J43-02	XMT+	
WHITE	J11-21	J43-03	RCV+	
-/——/-	J43-20	J43-06	DATA SET READY COMMONING STRIP SEE NOTE •	
WHITE	J11-22	J43-07	RCV-	
WHITE	J11-26	J42-01	TU0/1 PRES L	
WHITE	J11-27	J42-02	TU0/1 XMT-	
WHITE	J11-28	J42-03	TU0/1 XMT+	
WHITE	J11-29	J42-04	TU0/1 RCV+	
WHITE	J11-30	J42-05	TU0/1 RCV-	
WHITE	J11-34	J45-01	TU2/3 PRES L	
WHITE	J11-35	J45-02	TU2/3 XMT-	
WHITE	J11-36	J45-03	TU2/3 XMT+	
WHITE	J11-37	J45-04	TU2/3 RCV+	
WHITE	J11-38	J45-05	TU2/3 RCV-	
YELLOW	J11-45	J40-01	STATE LAMP L	
YELLOW	J11-46	J40-02	POWER ON L	
YELLOW	J11-47	J40-03	LAMP 0 L	
YELLOW	J11-48	J40-04	TERM ENA L	
YELLOW	J11-49	J40-05	LAMP 2 L	
YELLOW	J11-50	J40-06	LAMP 1 L	
YELLOW	J11-51	J40-07	LAMP 4 L	
YELLOW	J11-52	J40-08	LAMP 3 L	
YELLOW	J11-53	J40-09	SWITCH 1 L	
YELLOW	J11-54	J40-10	SWITCH 0 L	
YELLOW	J11-55	J40-11	SWITCH 3 L	
YELLOW	J11-56	J40-12	SWITCH 2 L	
YELLOW	J11-57	J40-13	BDCOK H (INT L)	
BLACK	J11-58	J40-14	GROUND	
RED	J11-60	J40-15	+5V	

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Figure 5-8 HSC50 Internal Cabling (2 of 5)

WIRE TABLE FOR 7019677-01				
COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	P41-1	P1-1	+12V	TU POWER
BLACK	P41-2	P1-3	GND (+12V)	TU POWER
BLACK	P41-3	P1-6	GND (+5V)	TU POWER
RED	P41-4	P1-5	+5V	TU POWER
WHITE	P42-1	P2-F	GND	TU SIGNAL
WHITE	P42-2	P2-D	RCV-	TU SIGNAL
WHITE	P42-3	P2-C	RCV+	TU SIGNAL
WHITE	P42-4	P2-J	XMT+	TU SIGNAL
WHITE	P42-5	P2-H	XMT-	TU SIGNAL
-/—/-	-/—/-	P2-E	-/—/-	KEYING PLUG (TU SIG)
YELLOW	P40-1	P3-1	STATE LAMP L	OCP
YELLOW	P40-2	P3-2	POWER ON L	OCP
YELLOW	P40-3	P3-4	LAMP 0 L	OCP
YELLOW	P40-4	P3-3	TERM ENA L	OCP
YELLOW	P40-5	P3-6	LAMP 2 L	OCP
YELLOW	P40-6	P3-5	LAMP 1 L	OCP
YELLOW	P40-7	P3-8	LAMP 4 L	OCP
YELLOW	P40-8	P3-7	LAMP 3 L	OCP
YELLOW	P40-9	P3-10	SWITCH 1 L	OCP
YELLOW	P40-10	P3-9	SWITCH 0 L	OCP
YELLOW	P40-11	P3-12	SWITCH 3 L	OCP
YELLOW	P40-12	P3-11	SWITCH 2 L	OCP
YELLOW	P40-13	P3-15	BDCOKH (INIT L)	OCP
BLACK	P40-14	P3-14	GND	OCP
RED	P40-15	P3-16	+5V	OCP
-/—/-	-/—/-	P3-20	-/—/-	KEYING PLUG (OCP)

WIRE TABLE FOR 7019679-01				
COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	J12-1	P31-1	+12V	
VIOLET	J12-2	P31-3	+12V	
VIOLET	J12-3	P31-5	+12V	
VIOLET	J12-4	P31-7	+12V	
BLACK	J12-5	P31-9	GND(+12V)	
BLACK	J12-6	P31-2	GND(+12V)	
BLACK	J12-7	P31-4	GND(+12V)	
ORANGE	J12-11	P31-6	-5V SENSE	TWISTED PAIR
BLACK	J12-12	P31-8	GND (-5V SENSE)	
BROWN	J12-13	P31-10	POWER FAIL	
-/—/-	J12-16	-/—/-	NO CONNECTION	KEYING PLUG
BLACK	J12-17	J32-1	GND (+5V SENSE)	TWISTED PAIR
RED	J12-18	J32-2	+5V SENSE	
BLACK	J12-19	J32-3	GND (+12V SENSE)	TWISTED PAIR
VIOLET	J12-20	J32-4	+12V SENSE	

WIRE TABLE FOR 7019680-01				
COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	J31-1	TB1-3-5	+12 V	DOUBLE CRIMP
VIOLET	J31-3			
VIOLET	J31-5	TB1-3-6	+12 V	DOUBLE CRIMP
VIOLET	J31-7			
BLACK	J31-9	TB1-3-3	GND (+12 V)	DOUBLE CRIMP
BLACK	J31-2			
BLACK	J31-4	TB1-3-3	GND (+12 V)	
ORANGE	J31-6	TB1-2-2	-5V SENSE	TWISTED PAIR
BLACK	J31-8	TB1-2-1	GND (-5V SENSE)	
BROWN	J31-10	TB1-1-4	POWER FAIL	

WIRE TABLE FOR 7019681-01				
COLOR	FROM	TO	SIGNAL	REMARKS
BLACK	P32-1	TB1-1-2	GROUND	TWISTED PAIR
RED	P32-2	TB1-1-1	+5V SENSE	
BLACK	P32-3	TB1-3-4	GROUND	TWISTED PAIR
VIOLET	P32-4	TB1-3-1	+12V SENSE	

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Figure 5-8 HSC50 Internal Cabling (3 of 5)

WIRE TABLE FOR 7019682-01

COLOR	FROM	TO	SIGNAL	REMARKS
-/-----/-	J13-2	-/-----/-	-/-----/-	KEYING PLUG
RED	J13-3	P50-1	+5V SENSE	TWISTED PAIR
BLACK	J13-4	P50-2	GND (+5V SENSE)	
BROWN	J13-5	P50-3	POWER FAIL	

WIRE TABLE FOR 7019683-01

COLOR	FROM	TO	SIGNAL	REMARKS
RED	J50-1	TB1-1	+5V SENSE	TWISTED PAIR
BLACK	J50-2	TB1-2	GND (+5V SENSE)	
BROWN	J50-3	TB1-4	PWR FAIL	

WIRE TABLE FOR 7019684-01

COLOR	FROM	TO	SIGNAL	REMARKS
BLACK	+V2	TB1-1	GROUND (-5V)	
BLACK	+V2	TB1-1	GROUND (-5V)	
BLACK	+V2	TB3-1	GROUND (-5V)	
BLACK	+V2	TB3-3	GROUND (-5V)	
ORANGE	-V2	TB2-3	-5 V	
ORANGE	-V2	TB3-2	-5 V	
ORANGE	-V2	TB4-1	-5 V	
ORANGE	-V2	TB5-3	-5 V	

WIRE TABLE FOR 7019686-01 STD PWR SUPPLY (60HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
GRN/YEL	GND STUD	J12•	GND	•POWER CONTROLLER J12
BLUE	TB1-2-7	J12•	ACC	
BRN	TB1-2-6	J12•	AC	

WIRE TABLE FOR 7019686-02 STD PWR SUPPLY (50HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
GRN/YEL	GND STUD	J5•	GND	•POWER CONTROLLER J5
BLUE	TB1-2-7	J5•	ACC	
BROWN	TB1-2-6	J5•	AC	

WIRE TABLE FOR 7019686-01 AUX PWR SUPPLY (60HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
GRN/YEL	GND STUD	J13•	GND	•POWER CONTROLLER J13
BLUE	TB1-7	J13•	ACC	
BROWN	TB1-6	J13•	AC	

WIRE TABLE FOR 7019686-02 AUX PWR SUPPLY (50HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
GRN/YEL	GND STUD	J6•	GND	•POWER CONTROLLER J6
BLUE	TB1-7	J6•	ACC	
BROWN	TB1-6	J6•	AC	

WIRE TABLE FOR 7019705-01

COLOR	FROM	TO	SIGNAL	REMARKS
-/-----/-	P4-01	-/-----/-	NO CONNECTION	SPARE
-/-----/-	P4-02	-/-----/-	NO CONNECTION	KEYING PLUG
RED	P4-03	D1-1	+5 V	
BLACK	P4-04	D1-2	GND (+5V)	
-/-----/-	P4-05	-/-----/-	NO CONNECTION	SPARE
YELLOW	P4-06	S1-4	GND	
YELLOW	P4-07	S1-5	TERM ENABLE	
-/-----/-	P4-08	-/-----/-	NO CONNECTION	SPARE
WHITE	P4-09	S1-1	INIT SWL	
WHITE	P4-10	S1-2	INIT L	

WIRE TABLE FOR 7020196-01

COLOR	FROM	TO	SIGNAL	REMARKS
YELLOW	S2-2	P33-4	ON/OFF (-5.3V)	
ORANGE	S2-1	P33-3	S2-	
BLUE	S2-4	P33-2	ON/OFF (+5V)	
BLACK	S2-5	P33-1	S1-	

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Figure 5-8 HSC50 Internal Cabling (4 of 5)

WIRE TABLE FOR 7020197-01

COLOR	FROM	TO	SIGNAL	REMARKS
YELLOW	J33-4	TB1-2-3	ON/OFF (-5.3V)	
ORANGE	J33-3	TB1-2-2	S2-	
BLUE	J33-2	TB1-1-3	ON/OFF (+5V)	DOUBLE CRIMP
BLUE	J34-2			
BLACK	J33-1	TB1-1-2	S1-	DOUBLE CRIMP
BLACK	J34-1			

WIRE TABLE FOR 7020198-01

COLOR	FROM	TO	SIGNAL	REMARKS
BLUE	J51-2	TB1-3	ON/OFF +5V	
BLACK	J51-1	TB1-2	S-	

WIRE TABLE FOR 7020199-01

COLOR	FROM	TO	SIGNAL	REMARKS
BLACK	P34-1	P51-1	S-	
BLUE	P34-2	P51-2	ON/OFF (+5V)	

WIRE TABLE FOR 7020200-01

COLOR	FROM	TO	SIGNAL	REMARKS
RED	A1-+	J70-1	-/------/-	
BLACK	A1-GND	J70-3	-/------/-	
WHITE	A1-LOAD	J7C-2	-/------/-	

WIRE TABLE FOR 7020201-01

COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	P70-1	K1-1	+12 V	DOUBLE CRIMP
VIOLET	P35			
ORANGE	P70-2	K1-6	LOAD (-5 V)	
ORANGE	P70-3	TB5-3	-5 V	

WIRE TABLE FOR 7020202-01

COLOR	FROM	TO	SIGNAL	REMARKS
WHITE	K1-3	P8-1	TRIP	
WHITE	K1-5	P8-2	RETURN	

WIRE TABLE FOR 7020203-01

COLOR	FROM	TO	SIGNAL	REMARKS
VIOLET	J35	TB1-3-2	+12 V	

WIRE TABLE FOR 7020206-01 (60HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
BLUE	J11•	P80-1	AC	• POWER CONTROLLER J11
BROWN		P80-2	AC	
GRN/YEL		P80-3	GROUND	
BLACK	P80-7	P80-4	-/------/-	JUMPER
BLACK	P80-6	P80-5	-/------/-	JUMPER

WIRE TABLE FOR 7020206-02 (50HZ)

COLOR	FROM	TO	SIGNAL	REMARKS
BLUE	J4 •	P80-1	AC	• POWER CONTROLLER J4
BROWN		P80-2	AC	
GRN/YEL		P80-3	GROUND	
BLACK	P80-5	P80-4	-/------/-	JUMPER

WIRE TABLE FOR 7020522-01

COLOR	FROM	TO	SIGNAL	REMARKS
RED	TB1-2	J46-2	+5 V	FROM BACKPLANE
BLACK	TB2-1	J46-1	GROUND	FROM BACKPLANE

WIRE TABLE FOR LINE CORD OF 7020613-01

COLOR	FROM	TO	SIGNAL	REMARKS
BROWN	X	LF1-PH3	-/------/-	LINE SIDE OF LF1.
BLACK	Y	LF1-PH2	-/------/-	
BLACK(2	Z	LF1-PH1	-/------/-	
BLUE	N	LF1-N	-/------/-	
GRN/YEL	GND	LF1-GND	-/------/-	

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Figure 5-8 HSC50 Internal Cabling (5 of 5)

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APPENDIX A
I/O PROCESSOR FUNCTIONAL DESCRIPTION

A.1 INTRODUCTION

The following paragraphs contain:

- P.ioc I/O page address utilization
- Interrupt and Trap location vectors
- I/O page register formats
- C connector pin assignments

A.2 P.IOC I/O PAGE ADDRESS UTILIZATION

PHYSICAL ADDRESS	FUNCTION
17 777 776	Processor Status Word
17 777 656	User PAR 7
17 777 654	User PAR 6
17 777 652	User PAR 5
17 777 650	User PAR 4
17 777 646	User PAR 3
17 777 644	User PAR 2
17 777 642	User PAR 1
17 777 640	User PAR 0
17 777 616	User PDR 7
17 777 614	User PDR 6
17 777 612	User PDR 5
17 777 610	User PDR 4
17 777 606	User PDR 3
17 777 604	User PDR 2
17 777 602	User PDR 1
17 777 600	User PDR 0
17 777 576	Memory Management Status Register 2
17 777 574	Memory Management Status Register 1
17 777 572	Memory Management Status Register 0
17 777 566	Console Xmtr Data Buffer Register
17 777 564	Console Xmtr Status Register
17 777 562	Console Rcvr Data Buffer Register
17 777 560	Console Rcvr Status Register

17 777 536	TU58 2 Xmtr Data Buffer Register
17 777 534	TU58 2 Xmtr Status Register
17 777 532	TU58 2 Rcvr Data Buffer Register
17 777 530	TU58 2 Rcvr Status Register
17 777 526	TU58 1 Xmtr Data Buffer Register
17 777 524	TU58 1 Xmtr Status Register
17 777 522	TU58 1 Rcvr Data Buffer Register
17 777 520	TU58 1 Rcvr Status Register
17 776 776)	
) >	Bootstrap PROM
17 773 000)	

A.3 P.IOC I/O PAGE ADDRESS UTILIZATION

17 772 516	Memory Management Status Register 3
17 772 356	Kernel PAR 7
17 772 354	Kernel PAR 6
17 772 352	Kernel PAR 5
17 772 350	Kernel PAR 4
17 772 346	Kernel PAR 3
17 772 344	Kernel PAR 2
17 772 342	Kernel PAR 1
17 772 340	Kernel PAR 0
17 772 316	Kernel PDR 7
17 772 314	Kernel PDR 6
17 772 312	Kernel PDR 5
17 772 310	Kernel PDR 4
17 772 306	Kernel PDR 3
17 772 304	Kernel PDR 2
17 772 302	Kernel PDR 1
17 772 300	Kernel PDR 0
17 770 056	Serial Number Register
17 770 054	Control Memory Low Address Register
17 770 052	Data Memory High Address Register
17 770 050	Data Memory Low Address Register
17 770 046	K Status Register
17 770 044	K Init Register
17 770 042	Switch/Display Register
17 770 040	Pio Control and Status Register
17 770 026	High Error Address Register
17 770 024	Low Error Address Register

17 770 022	Window Bus Register
17 770 020	Window Index Register
17 770 016	Window Address Register 7
17 770 014	Window Address Register 6
17 770 012	Window Address Register 5
17 770 010	Window Address Register 4
17 770 006	Window Address Register 3
17 770 004	Window Address Register 2
17 770 002	Window Address Register 1
17 770 000	Window Address Register 0
17 767 776))> 17 760 000)	Control Memory Windows

A.4 P.IOC INTERRUPT AND TRAP VECTORS

Numbers in parentheses indicate the order of priority of Level 4 interrupts.

ADDRESS	FUNCTION
000	(Reserved)
004	Bus error (nonexistent memory)
010	Control Error (nonexistent F-11 Control Chip)
024	Power Fail
060 (5)	Console Terminal, keyboard
064 (6)	Console Terminal, printer
100	Line Clock
114	Parity Error on read-from-memory
120 (7)	Control Bus Interrupt, Level 4
124	Control Bus Interrupt, Level 5
130	Control Bus Interrupt, Level 6
134	Control Bus Interrupt, Level 7
250	MMU abort
300 (1)	TU58 1, rcvr
304 (2)	TU58 1, xmtr
310 (3)	TU58 2, rcvr
314 (4)	TU58 2, xmtr

A.5 P.IOC I/O PAGE REGISTER FORMAT SUMMARY

WADR n (17 770 000 – 016)

(Write)

Double-Word Pointer (High 16 bits of 17-bit word address)

15 08 07 00

(Read)

1	1	1	0	n (0 – 7)	512-Byte Offset = Address of Low-Order Word of Double Word Pair

15 14 13 12 11 09 08 07 00

WINDR (17 770 020)

0	0	0	0	0	0	0	0	0	Window Index (000 – 177 (8))

15 08 07 06 00

WBUSR (17 770 022)

Double Word Pointer of Last Control Memory Reference

15 08 07 00

LOEADR (17 770 024)

Physical Address <15:00>

15 08 07 00

HIEADR (17 770 026)

0	0	0	0	0	0	0	0	0	0	Physical Address <21:16>

15 08 07 06 05 00

A.5.1 Control and Status Register (PIOCSR)

This register has the following format. Except as noted, all bits are Read/Write and are cleared by either Bus Init or IO Clear. This register is located at 17 770 040.

PIOCSR (17 770 040)

TRM ENA	0			SWP BRD	SWP BNK	SEL P 1	SEL P 0	ENA CBS	IO CLR	HIP TST	LOP TST	LED	NMA	CNT IE	LCK
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

where bit:	<15>	corresponds to the position of the front panel Secure/Enable switch. A one indicates the ENABLE position of the switch (Read-Only).
	<14>	Always zero.
	<13>	Not used.
	<12>	Not used.
	<11>	Swap Board, when set, causes the first two memory boards in the system to swap the base address for the private memory on each board.
	<10>	Swap Bank, when set, causes the first memory board in the system to swap the addressing ranges between private memory banks on that board. These two bits are provided to maximize the probability that working memory is available starting at address 000000 for interrupt vectors.
	<09:08>	Select P <1:0> provide a code which identifies which Control Bus interrupt field this P responds to. Both bits must be zero for the P.ioc.
	<07>	Enable Control Bus Arbitrator, when set, turns on the Control Bus Arbitrator for the seven other Control Bus requestors. When clear, only the P.ioc can access control memory.
	<06>	IO Clear, a Write-Only bit, is used to clear IO Page device registers.
	<05>	High byte Parity Test, when set, causes the high byte parity tree to generate even parity on the next Write cycle to memory, therefore writing incorrect high byte parity at that address. The bit is automatically cleared following that Write cycle. This function applies to all three areas of memory (program, control, and data). This bit is also cleared by Bus Init but not by IO Clear.
	<04>	Low byte Parity Test. Same as bit <05> but for the low byte.
	<03>	This bit lights a yellow LED (D6), located near the handle of the P.ioc, and also drives the STATE lamp located on the Operator Control Panel.
	<02>	Non-Memory Access, when set, causes the P.ioc to execute an NMA cycle on the next control memory or data memory access. This bit is cleared automatically at the conclusion of that control or data memory access. This bit has no effect on and is not cleared by program memory access.

<01> Control Memory Interrupt Enable, when set, causes the P.ioc to execute an interrupt cycle on the next control memory access. This bit is cleared automatically at the conclusion of that control memory access. Note, when the P.ioc accesses data memory with this bit set, the bit is cleared after that access with no interrupt generated.

<00> Control Memory Lock, when set, causes the P.ioc to execute a Lock cycle on the next control memory access. This bit is cleared automatically at the conclusion of that memory access. Note, when the P.ioc accesses data memory with this bit set, the bit is cleared after that access with no Lock cycle generated.

NOTE

These last three bits (NMA, CNT IE, and LCK) are prioritized so if more than one bit is set at a time, the highest priority bit determines which type of cycle occurs. Following that cycle, all set bits are cleared. The priority of these bits is:

1. **CNT IE**
2. **LCK**

A.5.2 Switch/Display Register (SWDR)

Software interface to the Operator Control Panel is through the Switch/Display register (SWDR), formatted as follows:

SWDR (17 770 042)

RESERVED	SW 3	SW 2	SW 1	SW 0	DIA OK	C/D NXM	INH PAR	LMP 4	LMP 3	LMP 2	LMP 1	LMP 0
15 12	11	10	09	08	07	06	05	04	03	02	01	00

where bits: <15-12> are reserved and are read as zeroes (Read-Only).

<11-08> are Read-Only and reflect the state of the corresponding switches on the Operator Control Panel. No hardware debounce circuitry is provided; debounce is a function of software.

<07> Completion of the diagnostics lights either a red LED (D7) or a green LED (D8), depending on module state. A zero lights the red LED and a one lights the green one. This bit powers up clear and is set to a one by the successful completion of the PROM bootstrap diagnostics. Once set, all modifications of this register must leave it set. This bit is a simple visual GO/NO-GO indicator for the P.ioc module.

<06> Control/Data Bus Nonexistent Memory test (C/DNXM), when set, forces an NXM trap on any Control or Data Bus access.

<05> Inhibit Parity Trap (INHPAR), when set, inhibits all parity traps, enabling examination of any memory location with a hard parity error.

<04-00> When set, lights the corresponding lamps on the Operator Control Panel (R/W).

These last eight writable bits are cleared by Host Clear, Bus Init, and IO Clear.

This register must be polled by software to detect changes in the state of the switches.

KINR (17 770 044)

K INIT <7:0>	SPARE	KST<3:0>
15 08	07 04	03 00

KSTR (17 770 046)

0	0	0	0	0	0	0	0	SP	STATUS
15							08	07	06 00

LODADR (17 770 050)

Data Bus Address <14:00>	0
15 08 07 01	00

HIDADR (17 770 052)

0	0	0	0	0	0	0	0	0	0	0	0	0	Data Addr <17:15>
15							08	07				03	02 00

LOCADR (17 770 054)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAD	0
15							08	07					02	01	00

S/NREG (17 770 056)

16-Bit Serial Number
15 08 07 00

TU58-1 RCSR (17 777 520)
TU58-2 RCSR (17 777 530)
TERM RCSR (17 777 560)

0	DEV PRS	0	0	0	0	0	0	RCV RDY	RCV IE	0	0	0	0	0	0
15	14						08	07	06						00

TU58-1 RBUF (17 777 522)
TU58-2 RBUF (17 777 532)
TERM RBUF (17 777 562)

ERR	OVR ERR	FRM ERR	0	0	0	0	0	RECEIVED DATA							
15	14	13					08	07							00

TU58-1 XCSR (17 777 524)
TU58-2 XCSR (17 777 534)
TERM XCSR (17 777 564)

0	0	0	0	0	0	0	0	XMT RDY	XMT IE	0	0	0	MNT	0	BRK
15							08	07	06				02		00

TU58-1 XBUF (17 777 526)
TU58-2 XBUF (17 777 536)
TERM XBUF (17 777 566)

0	0	0	0	0	0	0	0	TRANSMITTED DATA							
15							08	07							00

A.6 P.IOC C CONNECTOR PIN ASSIGNMENTS – EXTERNAL SIGNAL INPUTS

SIGNAL	PIN	PIN	SIGNAL
GROUND	C01	C02	−5.2V
+5V	C03	C04	+5V (B)
SNGL STEP L	C05	C06	BDAL 00 L
EXT HALT L	C07	C08	BDAL 01 L
PIOC ENA L	C09	C10	BDAL 02 L
Spare	C11	C12	BDAL 03 L
Spare	C13	C14	BDAL 04 L
Spare	C15	C16	BDAL 05 L
Spare	C17	C18	BDAL 06 L
TERM PRES L	C19	C20	BDAL 07 L
TERM XMT +	C21	C22	BDAL 08 L
TERM XMT –	C23	C24	BDAL 09 L
TERM RCV –	C25	C26	BDAL 10 L
TERM RCV +	C27	C28	BDAL 11 L
Spare	C29	C30	BDAL 12 L
Spare	C31	C32	BDAL 13 L
spare	C33	C34	BDAL 14 L
TU1 PRES L	C35	C36	BDAL 15 L
TU1 XMT +	C37	C38	BDAL 16 L
TU1 XMT –	C39	C40	BDAL 17 L
TU1 RCV –	C41	C42	BDAL 18 L
TU1 RCV +	C43	C44	BDAL 19 L
−5.2V	C45	C46	−5.2V
−5.2V	C47	C48	GROUND
TU2 PRES L	C49	C50	BDAL 20 L
TU2 XMT +	C51	C52	BDAL 21 L
TU2 XMT –	C53	C54	BRPLY L
TU2 RCV –	C55	C56	BSYNC L
TU2 RCV +	C57	C58	BDOUT L
MGN HI L	C59	C60	BDIN L
MGN LO L	C61	C62	BWTBT L
POWER ON L	C63	C64	BBS7 L
STATE LAMP L	C65	C66	BDCOK H (INIT L)
TERM ENA L	C67	C68	SWAP BRD H
LAMP 0 L	C69	C70	SWAP BNK H
LAMP 1 L	C71	C72	PREFR CLK L
LAMP 2 L	C73	C74	BINIT L
LAMP 3 L	C75	C76	POUT 0 L
LAMP 4 L	C77	C78	POUT 1 L
SWITCH 0 L	C79	C80	POUT 2 L
SWITCH 1 L	C81	C82	POUT 3 L
SWITCH 2 L	C83	C84	POUT 4 L
SWITCH 3 L	C85	C86	POUT 5 L
BPOK H (pwr fail)	C87	C88	POUT C H
−5.2V	C89	C90	−5.2V
+5V	C91	C92	+5V
GROUND	C93	C94	GROUND

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APPENDIX B
HSC50 REVISION MATRIX CHART

B.1 INTRODUCTION

Figure B-1 shows the revision status of all applicable HSC50 FRUs. An A1 HSC50 must have all the FRUs at a particular revision level in order to be supported.

HSC50 REVISION NUMBER					
			A1	B1	B2
FRU NAME	SLOT NO.	ETCH REV	MR/PR *	MR/PR *	MR/PR
L0100	14	C	D1		
L0105	1	D, E	D1	D1	D1, D2, E1
L0106-AH	2	C	C		
L0107-YA	12	C			
L0108-YA (HSC5X-BA)	4, 6, 7, 8, 9, 10	C	C2, C3, C4, C5		C6
		D	C2, C3, C4		C5
L0109	13	E	E1		
TU58-XA			OPTION REV F		
TU58-XB (54-13489)		E F	F1, F2, H, J, L		
OCP (54-15286)		B	B1		
BACKPLANE		E	E		

(Cont.)

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Figure B-1 HSC50 Revision Matrix Chart

HSC50 REVISION NUMBER					
			A1	B1	B2
FRU NAME	SLOT NO.	ETCH REV	MR/PR *	MR/PR *	MR/PR
MAIN POWER SUPPLY (70-20033) 60 HZ = 01 50 HZ = 02			L		
AUXILIARY POWER SUPPLY (70 20184) 60 HZ = 01 50 HZ = 02			J		
POWER CONTROLLER (70-19122) 60 HZ = 00 50 HZ = 01			B		
SYSTEM TAPE (BET492)			V100	V110 (C-DE)	
UTILITY TAPE (BET788C-DE)				V110	
INLINE DIAG TAPE (BET493)			V01-01	V110 (C-DE)	
TAPE KIT (00-ZD300-CG)			V100	V100	

* MR/PR = MODULE REVISION OR PART REVISION.

NOTE: THE 50 HZ VERSION OF THE HSC50 IS AVAILABLE STARTING WITH REVISION B1. BOTH THE HSC50 - AA (60 HZ) AND HSC50 - AB (50 HZ) ARE AT REVISION B1.

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Figure B-1 HSC50 Revision Matrix Chart

HSC50 GLOSSARY

ATTENTION – A message traveling from a storage device to the HSC50 or from the HSC50 to the host CPU. This message indicates a condition that should be brought to the attention of the higher ranking authority: the mass storage server or host CPU.

AUTOMATIC DIAGNOSTICS – Part of the HSC50 inline diagnostics, executed when testing detects an unacceptable level of errors.

AUXILIARY TERMINAL – A type of maintenance terminal used on the HSC50. This terminal is used to enter or display operating parameters for the HSC50 and to perform various diagnostics and utilities. It may be any EIA-compatible terminal set at 9600 or 300 baud. Currently, an LA12 terminal is shipped with the HSC50.

AVAILABLE – One state of a mass storage device used on the SDI/STI bus. When powered on, the device is considered available (but not online) to any controller in a configuration. The device is incapable of executing any online command until brought online by one of the HSC50s.

BLOCK – A stream of data transferred as a unit. Used interchangeably with the term *sector* for disk drives to represent 512 bytes (for 16- and 32-bit host architectures) or 576 bytes (for 36-bit architectures).

BLOCK DATA – One of the message delivery services of the System Communication Architecture. Block data messages are used for delivering fragments of data between host computers and HSC50s.

CI20 – DECSYSTEM 20 interface to the computer interconnect (CI) bus.

CI780 – VAX11/780 and VAX11/782 interface to the CI bus.

CI750 – VAX11/750 and VAX11/751 interface to the CI bus.

CI HOST INTERFACE (L0100) – A three-module interface including the port processor, the port buffer, and the port link modules.

CI LINK – Another term for the PORT LINK MODULE.

CLASS DRIVER – A Digital Storage Architecture (DSA) software driver residing in the host operating system. One class driver exists for each device class (disk or tape). The class driver functions are to convert the native I/O of the host operating system to Mass Storage Control Protocol (MSCP) or Tape Mass Storage Control Protocol (TMSCP) and to monitor the outstanding workload.

CLUSTER – A collection of processors called nodes, attached to each other by a high-speed bus. These processors are independent and survivable. They may be general purpose computers or special purpose servers, like the HSC50, providing a special set of services to the rest of the nodes.

COMMUNICATIONS SERVER – Part of the system interconnect architecture managing the communications side of a computer system. Communications servers can be:

- Terminal and unit record servers that connect to multiple DECnet systems on the Network Interconnect (NI, also known as ETHERNET).
- Routers that connect remote DECnet systems or other local area networks.
- Gateways that connect DECnet-based local area networks to foreign networks.

Communications servers offload functions from the central computer/software combination. The communications duties and capabilities they provide can be shared by Local Area Network hosts.

COMPUTE SERVER – Part of the system interconnect architecture; a hardware/software combination that manages the computation side of a computer configuration.

COMPUTER INTERCONNECT (CI) – The 70-Megabit/second/path dual path bus connecting the nodes in a cluster.

CONNECTION – The logical path in System Communication Architecture through which two processes communicate. Connections are multiplexed within a single virtual circuit.

CONTROL BUS – A path used by the various HSC50 modules to communicate with control memory. The bus is a 6 2/3 Megabyte per second pathway, multiplexed between the various memory requestors.

CONTROL MEMORY – One of the three HSC50 memories, containing 128 Kbytes of memory space. It is used for holding command packets and strings of orders to the drives as I/O requests pass through the HSC50.

CONTROL PROGRAM – An HSC50 software program stored on the System tape and loaded into program memory by a TU58. Also known as CRONIC, this program is responsible for governing all HSC50 operations.

CREDIT – Flow control mechanism for the System Communication Architecture. Two processes establishing a connection extend credit totals to each other indicating how many messages may be in process at any instant.

CRONIC – HSC50 control program found on the HSC50 System tape. It contains the programming instructions for HSC50 operation.

CYCLIC REDUNDANCY CHECK (CRC) – A checkword generally appended to a disk data transfer. This polynomial checksum is computed using data message bits as coefficients and dividing it by a generating polynomial. The resulting remainder is the CRC. When a transmitter computes and transmits a CRC following a data transfer, the receiver can recompute and compare it to verify correct reception. EDC and ECC, used by disks, are examples of CRC checkwords.

DATA CHANNEL – An HSC50 interface between the disk drive or tape formatters and HSC50 data memory. The HSC5X-BA is a disk data channel and the HSC5X-CA is a tape data channel.

DATA BUS – A pathway between HSC50 modules and data memory. A 13 1/3 Megabyte/second time-multiplexed bus, this bus permits reading, writing, and nonmemory access (NMA) cycles.

DATA MEMORY – One of three HSC50 memories, containing 128 Kbytes of memory space. All data transfers between the HSC50 and host computers or the HSC50 and peripheral devices is buffered in data memory.

DATAGRAM – One of the Port to Port Driver (PPD) packet delivery services used in the System Communication Architecture. A datagram is an unnumbered, self-contained message sent to a receiver with no delivery or sequencing guarantee. It is used for noncritical messages between the HSC50 and hosts. Examples are error log messages or messages reflecting drive state changes (such as a drive becoming ready).

DEVICE DRIVER – An operating system software module used to physically control an I/O device. In DSA, conventional device drivers are replaced by a single driver for an entire class of devices, such as disk drives, and a single port driver for the host to controller transport mechanism. A host computer communicating with the HSC50 uses disk and tape class drivers and the CI port driver.

DIAGNOSTIC AND UTILITY PROTOCOL (DUP) – A system application level protocol used by a host computer. DUP directs an HSC50 to run internal diagnostics or utility functions. It is implemented as a class driver on the host and a corresponding server on the HSC50.

DIGITAL STANDARD DISK FORMAT (DSDF) – The Digital Storage Architecture standard for disk media format. It specifies the mechanism for mapping a contiguous logical block address space into a possibly imperfect physical space, as well as defining diagnostic and factory areas. DSDF is transparent to the systems.

DIGITAL STORAGE ARCHITECTURE (DSA) – A set of specifications and interfaces describing standards for designing mass storage products. DSA defines the functions performed by host computers, controllers, and drives. It also specifies how they interact to accomplish mass storage management.

DISK BACKUP – Disk backup is the copying of information from disk to tape for data protection. An HSC50 utility program (BACKUP) provides for HSC50-instigated backup involving neither the CI bus nor the host memory. This local backup process is given a low-level priority to avoid interference with HSC50 operation. Backup can be run offline to the cluster with the HSC50 executing the entire operation.

DISK DATA CHANNEL MODULE (L0108-YA) – Part of the data path to the disk drives. Among its functions, this module transmits data between the HSC50 data memory and the disk drives, transmits control and status information to the drives, and monitors real-time status information from the drives.

DISK SHADOWING – Copying data to two or more additional disk drives. The HSC50 manages disk shadowing internally. When a host computer declares a set of identical disk drives is a shadow set, the drives are treated as one from the host point of view. The HSC50 writes all data to all drives in the shadow set and selects the optimum drive for reading. Shadowing is done on a volume basis.

DISTRIBUTED LOCK MANAGER – The VMS mechanism for synchronizing access to files and records shared between host CPUs in a cluster.

DUAL PORTING (or DUAL ACCESS) – Ability of a disk or tape drive to be accessed by two controllers. All DSA drives have a standard dual port feature. DSA drives can be online to only one controller at a time. However, they are able to disconnect themselves from a failed controller and become available for continued service through the other controller.

ERROR CORRECTION CODE (ECC) – A CRC that recognizes a mismatch between transmitted and computed code. ECC can determine the location of an error in the message and correct data. All ECCs have limited correction power. The ECC used by DSA drives is 170 bits long with a maximum correction power of 80 bits per sector in 8 separate bursts.

ERROR DETECTION CODE (EDC) – A shifted checksum applied to blocks of data stored on DSA devices. The EDC is ECC checked and serves as a check on ECC logic and controller internal data paths. Every element of the HSC50 that manipulates data blocks verifies correct EDC.

ETHERNET – The industry standard term for the DIGITAL Network Interconnect (NI).

EXTENDED HEX MODULE – A printed circuit board 11 inches wide by 17 inches high. It is the largest of the standard circuit modules available from DIGITAL.

FIRMWARE – PDP-11 code loaded in the HSC50 from the TU58 tape. It differs from microcode because it is loadable and the PDP-ll, on which it executes, is a vertical machine.

FORCED ERROR FLAG – Complement of the EDC. This flag is used to indicate a data block probably contains incorrect data.

FORMAT CONTROL TABLE (FCT) – Records information concerning the location of manufacturing-detected bad blocks on the disk. It also identifies the current mode of the logical block space (512 or 576 byte).

HORIZONTAL MICROCODE – Microcode for microprocessors with architecture permitting multiple conventional instructions in a single instant of time. All HSC50 microprocessors (except the master control microprocessor) are designed for horizontal microcode.

HSC50 – An intelligent mass storage server used on the Computer Interconnect (CI) bus. Capable of supporting a total of six disk and/or tape data channels, the HSC50 is part of the System Interconnect Architecture and DIGITAL Storage Architecture. By performing as an I/O manager, the HSC50 can be classified as an I/O server, removing the burden of I/O management from the CPU.

INLINE DIAGNOSTICS – Diagnostics running in parallel with normal I/O operations, requiring dedication only of those resources under diagnosis. Some run automatically within the HSC50 and others are operator-initiated from the TU58 Utilities and System tapes.

INPUT/OUTPUT CONTROL PROCESSOR MODULE (L0105) – Primarily responsible for controlling HSC50 internal operations. The module logic contains a PDP-11 processor that operates from a control program loaded from a TU58 tape and stored in program memory.

I/O SERVER – A processor occupying the position of controller within the DSA or DNA but offering substantially more function and performance than the conventional controller. The HSC50 is an I/O server.

K.ci MODULE – Same as the CI HOST INTERFACE.

K.pli MODULE – An engineering term for the PORT PROCESSOR MODULE.

K.sdi MODULE – An abbreviation for the DISK DATA CHANNEL.

K.sti MODULE – An abbreviation for the TAPE DATA CHANNEL.

LOCAL AREA NETWORK – A cluster of servers communicating over the Network Interconnect.

LOGICAL BLOCK – The entity by which DSA disk data is organized as perceived by the host computer. The size of a logical block can be either 512 or 576 bytes.

MANAGER – An HSC50 process responsible for controlling a particular interface such as disk, tape, or the CI. Managers are comparable to CPU operating system drivers.

MANCHESTER ENCODING – A technique for high-speed serial data transmission. It is self-clocking and minimizes error probability through frequent channel state transitions. The CI bus uses Manchester Encoding.

MASS STORAGE CONTROL PROTOCOL (MSCP) – The message level protocol used by a DSA controller to communicate with its host computer. The three types of MSCP communication are sequential messages, datagrams, and block data transfers. Both the HSC50 and the UDA50 UNIBUS use MSCP.

MASS STORAGE SERVER – An I/O server specifically for disk and tape drive control. The HSC50 is such a server.

MEMORY MODULE (L0106-AA) – Contains three memories: data memory (M.dat), program memory (M.prog), and control memory (M.ctl).

MODULARITY CONNECTORS – Jumpers the SC008 Star Coupler panels together. This allows creation of parallel, redundant paths for the CI.

MSCP SERVER – Processes MSCP host commands, passes the commands to HSC50 device-specific modules, and sends responses to host commands back to the issuing class driver.

M.std – An engineering term for the MEMORY MODULE.

NETWORK INTERCONNECT (NI) – One of two standard interconnects used in the System Interconnect Architecture. (The Computer Interconnect is the other.) The NI (also known as ETHERNET) connects communications servers and compute servers creating a local area network.

NODE – Intelligent entities in a distributed computing configuration. Nodes are independent but linked, as in a network or a cluster, becoming parts of a whole. In a cluster, HSC50s and host computers are cluster nodes.

OFFLINE – One of the possible status conditions of a mass storage device or server. When a device is offline, it is not capable of communicating with the controller. When the controller is offline, it is inaccessible to any node in the configuration.

OFFLINE DIAGNOSTICS – Diagnostics executed only in an offline state. Such diagnostics require HSC50 dedication and cannot run parallel with normal I/O operations.

OFFLINE DIAGNOSTICS TAPE – TU58 tape containing the Offline diagnostics for the HSC50.

PERIODIC DIAGNOSTICS – Diagnostics run in HSC50 idle time. They are initiated by internal timers and do not disrupt normal I/O operations. When enabled by the SET PERIODIC DIAGNOSTICS command, these diagnostics run by default, testing the disk data channel, the tape data channel, and memory.

PHYSICAL INTERCONNECT – Physical layer of the System Communication Architecture. It incorporates the electrical specifications for the CI bus, as well as the arbitration mechanism, packet framing, and error recovery.

PILA MODULE – An engineering term for the PORT BUFFER MODULE.

P.ioc MODULE – An engineering term for the I/O CONTROL PROCESSOR.

POLLER – A process which, by convention, runs in each node of a cluster. Its function is to recognize and connect to new nodes as they appear on the cluster, thereby supporting dynamic reconfiguration.

PORT – The hardware and software used to connect a host or controller to a communication bus (such as the CI bus or SDI bus).

PORT BUFFER MODULE (L0109) – One of the three modules constituting the HSC50 CI interface. This module contains scratchpad buffers for packets received or transmitted on the CI bus.

PORT DRIVER – In the DSA or the SCA, an operating system program concerned with delivery of packets rather than their contents.

PORT LINK MODULE (L0100) – One of the three modules making up the HSC50 CI interface. This module is the HSC50 direct interface to the CI bus.

PORT/PORT DRIVER (PPD) – The message delivery level protocol of System Communication Architecture.

PORT PROCESSOR MODULE (L0107) – The microprocessor module in the HSC50 CI interface. Any data coming from a host is routed to HSC50 memory by the port processor module. Any data coming from HSC50 memory enroute to a host is also controlled by the port processor module.

PROGRAM MEMORY – One of three HSC50 memories. It is 256 bytes long, and used to store the firmware run by the HSC50 master control microprocessor. Program memory is protected by byte parity checking, and bad sections of memory are excluded from use.

READ/WRITE READY – One of the four status bits obtained in the real-time drive state message on the SDI/STI bus. When Read/Write Ready is asserted, the mass storage device is capable of handling a data transfer to or from the media. Any disk positioning or tape motion negates this signal.

RECEIVER READY – One of the status bits used on a DSA device. When Receiver Ready is active, the device can receive a command from the controller. The bit negates while the device processes the command. The same is true of the controller (UDA50, HSC50). The controller is ready to receive messages from the host when Receiver Ready is active.

REPLACEMENT – An algorithm defined by DSA. Defective or potentially defective sectors are removed from service and replaced by others reserved for that purpose on the volume. Replacement and revectoring allows a host computer to perceive every DSA volume as logically perfect.

REPLACEMENT AND CACHING TABLE (RCT) – Contains information about the state of any disk replacement or formatting operation completed or in progress. A copy of the volume serial number is also contained in this table to allow RCT validation by the diagnostics.

REQUESTOR – A generic term for entities in the HSC50 which access data memory. Requestors include all data channels, the port processor, and the I/O control processor.

RESTORE – Data previously backed up on tape is retrieved for disk storage using the normal priority. Backup is used to preserve information in the event of a disk failure. Restore is used to recover the information.

REVECTOR – An algorithm defined by DSA by which a controller (without host intervention) can locate replaced sectors on a disk volume.

SECTOR – The physical entity for organizing data on a disk surface. A sector includes either 512 bytes (for 16- and 32-bit host architectures) or 576 bytes (for 36-bit architectures) of user data, plus a quadruplicated header, an EDC, and an ECC for data integrity.

SEEK – The process of moving the Read/Write heads of a disk drive to the radius where the desired data resides.

SEQUENCED MESSAGE – One of the message delivery services of the System Communication Architecture. These messages are used to communicate commands and status responses between host computers and HSC50s.

SERVER – Either the HSC50 (refer to MASS STORAGE SERVER) or a SYSAP level process in the HSC50. This process is responsible for communication with a host computer class driver. Disk, Tape, and Diagnostic and Utilities Protocol (DUP) servers are found in the HSC50.

STANDARD DISK INTERFACE (L0108-YA) – The DSA standard for connecting disk drives and controllers. An SDI bus connects each drive to the controller in a parallel configuration. The standard disk interface is a 4-line radial bus, one for each of the following functions: transfer of serial data from the HSC50 to the disk, transfer of serial data from the disk to the HSC50, transfer of serialized status signals from the drive to the HSC50 and transfer of serialized status signals from the HSC50 to the disk.

STANDARD TAPE INTERFACE (L0108-YB) – The DSA standard for connecting tape formatters and controllers. An STI bus connects each tape formatter to the HSC50 in a parallel configuration. The standard tape interface is a 4-line radial bus. One line each is used for transfer of serial data to the tape formatter from the HSC50 and to the HSC50 from the formatter. One line each is used for transfer of serialized status signals to the HSC50 from the tape formatter and one is used for transfer of such signals from the HSC50 to the formatter.

STAR COUPLER – The physical hub of a cluster. The Star Coupler (SC008) is a cabinet containing cable connectors and transformers where all the nodes of a cluster are connected to each other.

SURVIVABILITY – The ability of connected computers to continue functioning properly after the failure of one. Survivability of nodes is a fundamental property of clusters.

SYSTEM COMMUNICATION ARCHITECTURE (SCA) – The interface specifications and protocols defining the connection of independent computer systems into clusters.

SYSTEM TAPE – A TU58 tape containing the control program (CRONIC) governing HSC50 operation. Also, two inline diagnostics, the TU58 Inline Test and the Inline Memory Test, are located on the System tape.

THROUGHPUT – The amount of user data passing over a bus or across an interface per unit of time. Throughput is usually an average of a fairly long period, such as a second.

TAPE MASS STORAGE CONTROL PROTOCOL (TMSCP) – An applications protocol used by the HSC50 to communicate with the host computer. It is tape specific, but overlaps and shares certain portions of MSCP.

TRANSFER RATE – The rate at which signaling entities pass over a bus or across an interface.

TRANSFORMER COUPLING – Connection of a transmission cable to an interface using transformers rather than physical contact so the ends of the transmission cable do not require a common ground reference.

UDA50 – An SDI controller that operates on the UNIBUS under MSCP protocol. The UDA50 can support a maximum of four disks communicating over the SDI bus.

UTILITIES – Programs enabling the user to change HSC50 characteristics, obtain status, and perform such functions as backup, format, and verify. These programs are found on the Utilities tape, one of three TU58 tapes shipped with the HSC50.

VIRTUAL CIRCUIT – A logical connection path between two nodes in a cluster. The message traffic of the communicating processes is multiplexed using this circuit as an envelope.

VOLUME SHADOWING – Refer to DISK SHADOWING.

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